MLSoC™ PCIe HHHL Board Hardware Reference Manual

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Table of Contents

List of Figures 6
List of Tables 7
Revision History 9
About this Document 11
iv.1 Purpose and Scope 11
iv.2 Intended Audience 12
iv.3 Known Issues 12
iv.4 Reference Documentation 12
iv.5 List of Acronyms 13
Chapter 1 General Safety Guidelines and Precautions 15
Chapter 2 Overview 16
2.1 Architecture 16
2.2 PCIe HHHL Board Features 18
2.2.1 Board Dimensions (Form Factor) 18
2.2.2 Board Operating Conditions 18
2.3 PCIe HHHL Board Interface Description 18
2.3.1 MLSoC Architecture 18
2.3.2 MLSoC Power Requirements 19
2.3.3 Power Up Sequencing 19
2.4 MLSoC Interfaces 20
2.4.1 Single PCIe HHHL Board Specifications 20
2.4.2 LPDDR4 Interface (32-Bit) 20
2.4.3 MLSoC eMMC Interface 24
2.4.4 MLSoC I2C Interface 25
2.4.5 Ethernet Interface 27
2.4.6 MLSoC UART Interfaces 30
2.4.7 JTAG Interface 32
2.4.8 MLSoC SPI-8 Interface 33

2.4.9 GPIO Interface 34
2.4.10 PCIe Interface 37
Chapter 3 Clock Requirements 40
3.1 Clock Requirements 40
Chapter 4 Power and Reset 41
4.1 Power Requirements 41
4.1.1 Circuit Protection 41
4.1.2 Power Tree 41
4.2 Main Buck Regulator for Generating 3.3V @ 24A 42
4.3 Buck Regulator for MLSoC Core Voltage 0.85V @ 40A 42
4.4 Buck Regulator for LPDDR4 Controller VDDQ Voltage and LPDDR4 IC 1.1V @ 3A .. 42
4.5 Buck Regulator for MLSoC IO Voltages, LPDDR4 VDD, eMMC VDDQ 1.8 @ 3A 42
4.6 Reset 43
Chapter 5 Operation and Maintenance 44
5.1 LED Features 44
5.2 Test Points 44
Chapter 6 PCB and Packaging 45
6.1 PCB Dimensions 45
6.2 Board Layer Description 45
Chapter 7 Signal and Power Integrity Analysis 46
7.1 Pre-layout SI Analysis 46
7.2 Post Layout SI Analysis 46
7.3 PI Analysis 46
7.4 Thermal Analysis 47
Chapter 8 Certification Data 49
8.1 Summary of Test Results 49
8.1.1 Emissions 49
Chapter 9 Environmental and Compliance Specifications 52
9.1 Environmental Requirements 52
9.2 Environmental Specifications 52

9.3 EMI/EMC and Other Compliance 52
Chapter 10 Support 53

List of Figures

Figure 2-1. PCIe HHHL Board Top View 16
Figure 2-2. PCIe HHHL Board Functional Block Diagram 17
Figure 2-3. PCIe HHHL Board Power Up Sequencing Implementation 19
Figure 2-4. MLSoC to LPDDR4 Interface 22
Figure 2-5. MLSoC eMMC Interface 24
Figure 2-6. MLSoC I2C Interface 26
Figure 2-7. MLSoC Ethernet Interface 28
Figure 2-8. MLSoC UART Interface 31
Figure 2-9. MLSoC JTAG Interface 32
Figure 2-10. MLSoC SPI-8 Interface 34
Figure 2-11. MLSoC GPIO Interface. 35
Figure 2-12. x8 PCIe Gen 4 Interface Functional Block Diagram 38
Figure 4-13. System Reset 43

List of Tables

Table iv-1. Reference SiMa.ai Documents 12
Table iv-2. Additional Documents 12
Table iv-3. Acronyms 13
Table 2-1. MLSoC Power Requirements 19
Table 2-2. PCIe HHHL Board Specifications 20
Table 2-3. LPDDR4 Power Requirement Per Device 21
Table 2-4. LPDDR4 Interface Signal Pin-outs 23
Table 2-5. Power Requirement for eMMC Flash IC 24
Table 2-6. MLSoC eMMC Interface Pin-out 25
Table 2-7. I2C PCIe HHHL Board Pin-out 26
Table 2-8. Power Requirements for MLSoC Ethernet PHY 28
Table 2-9. Eth0 PHY Mode and Address Configuration 29
Table 2-10. Eth1 PHY Mode and Address Configuration 29
Table 2-11. Ethernet Interface Pin-outs 30
Table 2-12. UART Interface Pin-outs 31
Table 2-13. UART Connector Pin-outs 31
Table 2-14. MLSoC JTAG Pin-outs 32
Table 2-15. MLSoC JTAG Connector Pin-outs 33
Table 2-16. MLSoC Quad SPI Programming Header Pin-outs 34
Table 2-17. MLSoC GPIO Interface Pin-outs 35
Table 2-18. MLSoC PCIe Gen 4 x8 Dual PCIe HHHL Board Edge Connector Pin-outs 38
Table 3-1. Clock Requirements 40
Table 5-1. LED Requirements 44
Table 6-1. PCB 12 Layer Stack-up 45
Table 8-1. Emissions 49
Table 8-2. Immunity Results 50

Revision History

The following table provides a history of changes made to this document.

Date	Version	Description
May 15, 2023	A	• Initial release.
August 31, 2023	B	Updated **Known Issues** and added information on how to access SiMa.ai Developer Zone. • Replaced photographs. • Modified **Chapter 1.** • Made major changes in **Chapter 2.** • Modified power requirements in **Table 2-1. MLSoC Power Requirements**. • Modified Operating temperature range in **Table 2-2. PCIe HHHL Board Specifications**. • Modified **Section 2.4.2 on page 20**. • Modified **Section 2.4.3 on page 24**. • Modified **Figure 2-4. MLSoC to LPDDR4 Interface on page 22**. • Modified **Figure 2-5. MLSoC eMMC Interface on page 24**. • Modified **"Table 2-6. on page 25"**. • Modified cross-reference description of **Figure 2-7. MLSoC Ethernet Interface on page 28**. • Modified the PCI reference clock bullet in **Section 2.4.10**. • Modified **Section 2.4.10 on page 37**. • Modified **"Table 3-1. on page 40"**. • Modified Buck regulator voltage values in **Chapter 4.** • Removed Power Tree figure and table from **Chapter 4, Section 4.1.2. Power Tree**. • Modified **Section 6.1 on page 45**. • Replaced Figure 8-2. PCIe HHHL Board Placement (Bottom) on page 51.
October 16, 2023	C	Made the following changes: • Updates per editorial review (example: publish date, revision number, formatting) • Updates per technical review (example: removed chapter on PCIe HHHL card placement plan, removed reference to TVM and Netron software tools)

About this Document

SiMa.ai's Machine Learning System on Chip (MLSoC) delivers high-performance, effortless machine learning inference for embedded edge applications. Built on 16nm technology, the MLSoC's processing system consists of a computer vision processor, coupled with dedicated Machine Learning Acceleration (MLA) and high-performance application processor. Surrounding various processors are memory interfaces, communication interfaces, and system management, all connected via a network on chip (NoC).

The SiMa.ai MLA IP is the core of the SiMa.ai MLSoC which provides a platform for accelerating next generation machine learning applications.

NOTE! Signal direction and IO types mentioned in the pin-outs are defined with respect to the MLSoC device.

iv.1 Purpose and Scope

This document provides detailed design and hardware reference information for the PCIe HHHL Board using the SiMa.ai MLSoC device. It includes PCIe implementation, block level functional description of each interface, power requirements, clock tree, reset sequence, and PCB characteristics.

It covers the following topics:

- General safety guidelines and precautions
- Board overview
  - Configuration details
  - Board architecture and interface details
- Power requirements
- Board specifications
- Clock requirements
- Power tree and reset sequence
- Operation and maintenance features
- SI and PI Thermal Analysis
- Environmental & compliance, and
- Technical support

iv.2 Intended Audience

This document is intended for HW/System engineers who are interested in deploying PCIe HHHL Card into their design. It also serves as a reference for designers who wants to design their own PCB/board with SiMa's MLSoC chip. An advanced knowledge of high-speed circuit/PCB design, memory interfaces, and familiarity with various Ethernet, PCIe-based designs is required.

iv.3 Known Issues

This document contains the following errors/known issues. These will be addressed and resolved in a future release.

- **Issue**: Significantly small font size for labels in the block diagram in Figure 2-3 affects readability.

  Solution: Select the diagram and zoom out to enlarge the font size.

iv.4 Reference Documentation

These documents provide additional information in understanding the SiMA.ai MLSoC and the Palette software platform (also called the SDK).

Table iv-1. Reference SiMa.ai Documents

Document Name	Description
MLSoC™ SM1 Datasheet	Provides product overview and architectural overview of MLSoC SM1. In addition, it provides pinout information, electrical specifications, thermal specifications, packaging information, and ordering information.
MLSoC™ Evaluation Board Hardware Reference Manual	Serves as a reference for the designers who want to design their own PCB/board with SiMa.ai's MLSoC chip.
MLSoC™ PCIe Half-height, Half-length Production Board Product Brief	Describes the key features of this product, interfaces, and functional block diagram of the Half-length Board Production Board.
MLSoC™ (Machine Learning System on Chip) Product Brief	Provides MLSoC highlights, overview and architecture features. It covers basic power on, reset, and clock test procedures, SPI configuration, and board interfaces.
MLSoC™ Evaluation Board Product Brief	Describes key features of the MLSoC. In addition, it provides a functional block diagram that shows all the major blocks of the MLSoC Evaluation Board.
Palette™ Developer User Guide	Describes the SiMa.ai's Palette software platform including how to compile, build, and deploy real-time applications, in conjunction with the MLSoC Evaluation Board. Additionally, the developers can debug, evaluate performance, and fine-tune applications.
Palette™ Product Brief	Introduces the SiMa.ai's Palette software platform which is designed for complete ML stack application development.

Table iv-2. Additional Documents

Internal/External URL Link for Additional Document	Description
1. https://developer.sima.ai/	Developer Zone for SiMa.ai customers. Request access for the latest software download and documentation by sending email to: **developer.mlsoc@sima.ai**

iv.5 List of Acronyms

The following acronyms are used in this document.

Table iv-3. Acronyms

Acronym	Description
DFM	Design for Manufacturability
DFT	Design for Testability
DRAM	Dynamic Random-Access Memory
EMI	Electromagnetic Interference
eMMC	Embedded Multi Media Card
ESD	Electrostatic discharge
HHHL	Half Height Half Length
Gbps	Giga Bits Per Second
GPIO	General Purpose Input Output
I^2C	Inter Integrated Circuit
IBIS	IO Buffer Information Specification
IC	Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
MB	Mega Byte
MHz	Mega Hertz
MLSoC	Machine Learning System on Chip
mm	Millimeter
MDIO	Management Data Input/Output
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCIe HHHL	Peripheral Component Interconnect express Half Height Half Length card, also known as industry standard PCIe Low Profile card.
PD	Power Delivery
PI	Power Integrity
PMIC	Power Management Integrated Circuit
POS	Position

Table iv-3. Acronyms

Acronym	Description
QSPI	Quad Serial Peripheral Interface
R/A	Right Angled
RoHS	Restriction of Hazardous Substances
SBC	Single Board Computer
SD	Secure Digital
SGMII	Serial Gigabit Media-Independent Interface
SI	Signal Integrity
SMD	Surface Mount Device
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TBD	To Be Determined
UART	Universal asynchronous receiver-transmitter
USB	Universal Serial Bus

Chapter 1
General Safety Guidelines and Precautions

This chapter provides general safety guidelines and precautions when handling the PCIe HHHL Board and working with electricity in order to avoid any damage to the board and personal injury.

CAUTION! Follow these safety precautions and warnings. Failure to comply may result in damage to the board.

- Use proper ESD grounding techniques when handling the board.
- Wear an antistatic wrist strap and use an ESD-protected mat.
- Do not touch the board in power on state.
- Store the board in an antistatic bag before placing it on any surface.
- Handle the module from the edges and avoid touching any of the onboard ICs/components.
- Do not connect any higher I/O voltage level signals than specified in the SM1 Datasheet.
- Use the appropriate power supply that is supplied with the module.
- After power on, make sure all the power indication LEDs are lit.

WARNING! Use the following safety precautions. Failure to comply may result in damage to the board and/or result in personal injury.

- Boards are not conformal coated and can get damaged due to water or any other conductive liquids. Keep water and other conductive liquids away from the PCIe HHHL Board.

Chapter 2
Overview

- Designed to meet the highest performance, low power, and safe and secure machine learning applications using the MLSoC.
- Supports PCIe Gen 4.0 x8 interface, I2C, SPI-8, 1G Ethernet, JTAG, UART, LPDDR4, and GPIO interfaces.
- The board form factor is PCIe Half Height Half Length and it has a board edge connector for PCIe x8 interface of 98 pins in the south edge of PCB.

Figure 2-1. shows the top view of the PCIe HHHL Board.

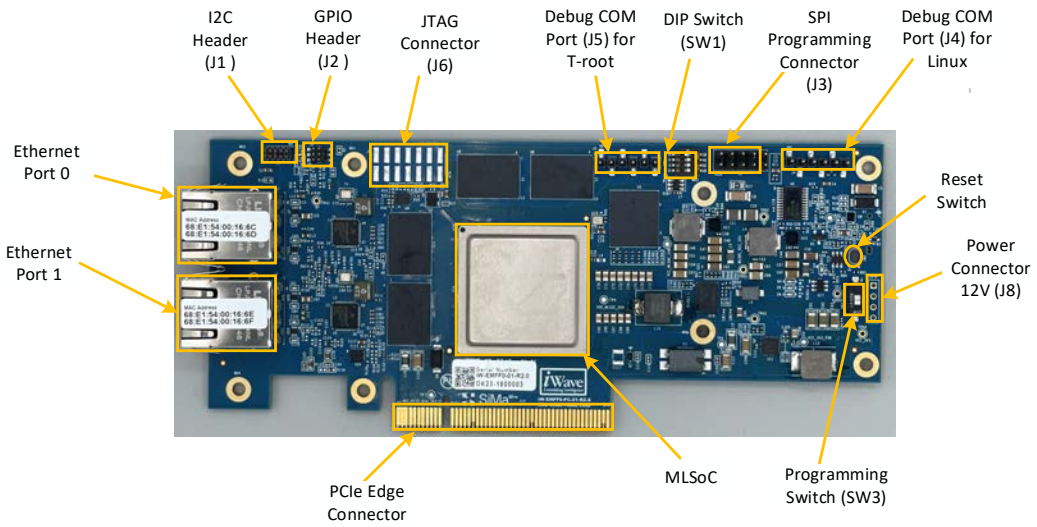

Figure 2-1. PCIe HHHL Board Top View

2.1 Architecture

The PCIe HHHL Board was designed using the MLSoC SM1 chip. Its high-level architecture functional block diagram is shown in **Figure 2-2.**

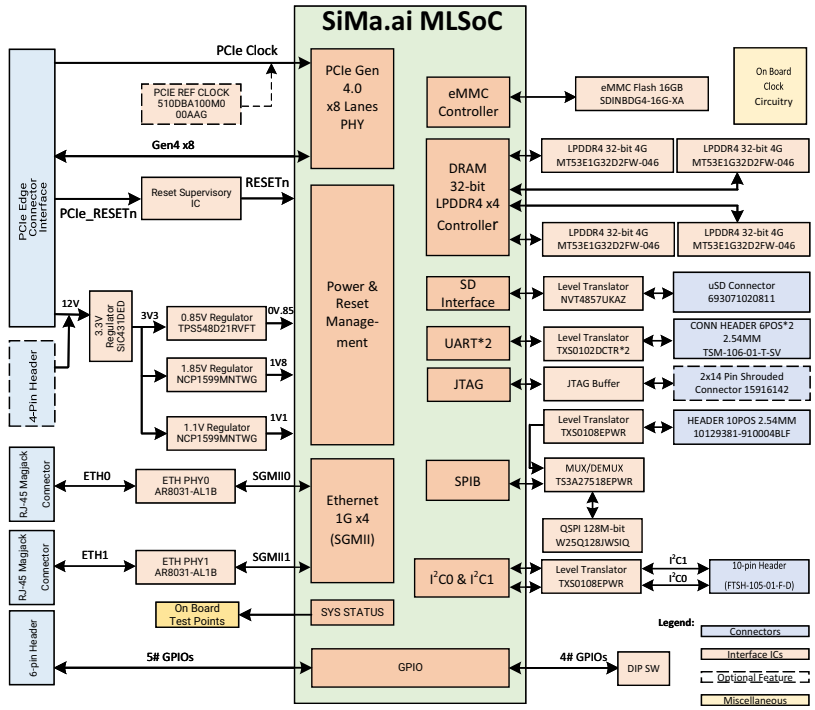

Figure 2-2. PCIe HHHL Board Functional Block Diagram

CAUTION! Do not use the board for any purpose other than its intended use because it is programmed for its intended use.

2.2 PCIe HHHL Board Features

- 1x of PCIe Gen 4.0 x8 link interface with standard board edge connector in PCIe HHHL card configuration
- 4 x 4GB 32Bit LPDDR4 DRAM Interface
- 1 x 16GB eMMC Flash Memory Interface
- 1 x 128Mbit QSPI NOR Flash Interface
- 2 x 1Gbps Ethernet on RJ45
- 2 x I2C Interfaces with header
- 1 x JTAG Interface (optional)
- 1 x Micro SD Interface
- 1 x Debug UART for Troot
- 1 x Debug UART for Linux.

2.2.1 Board Dimensions (Form Factor)

- Form Factor (single slot width): 160mm (L) x 68.9mm (H) standard PCIe HHHL Board

2.2.2 Board Operating Conditions

- 0°C to 70°C (commercial grade)

2.3 PCIe HHHL Board Interface Description

2.3.1 MLSoC Architecture

SiMa.ai MLSoC is the main processor for PCIe HHHL Board. Following are the details of the PCIe HHHL Board chip set:

- Part Number:
  - MLSoC-Pro-16GB-114-ADA (MLSoC Production Board - PCIe HHHL Industrial 50 TOPS)
  - MLSoC-Pro-16GB-116-ABA (MLSoC Production Board - PCIe HHHL Commercial 50 TOPS)
- DRAM Controller: 4 x 32-bit DRAM
- PCIe blocks: 1x PCIe Gen4.0 x8 lanes
- Ethernet block: 2 x 1Gbps SGMII MAC to PHY
- Total Number of IOs: 31GPIOs are available, but only 23 of them are used in the design.
- Package: 1369-ball high performance BGA (FCBGA) package
- MLSoC temperature grade:
  - 0°C to 70°C (Commercial grade)
  - –40°C to +85°C (Industrial grade)

2.3.2 MLSoC Power Requirements

Table 2-1. MLSoC Power Requirements

Power Rail	Typical Voltage	Tolerance	Selected Regulator Max Current Output (A)
MLSoC_Core	0.85V	–7% to +10%	40
VDDIO	1.8V	–7% to +10%	3
VDDQ	1.1V	–7% to +10%	3

2.3.3 Power Up Sequencing

The MLSoC and memory interface supply voltages are powered up by separate regulators than the ones used for generating power supply for other on-board circuitries. **Figure 2-3.** shows the power up sequences.

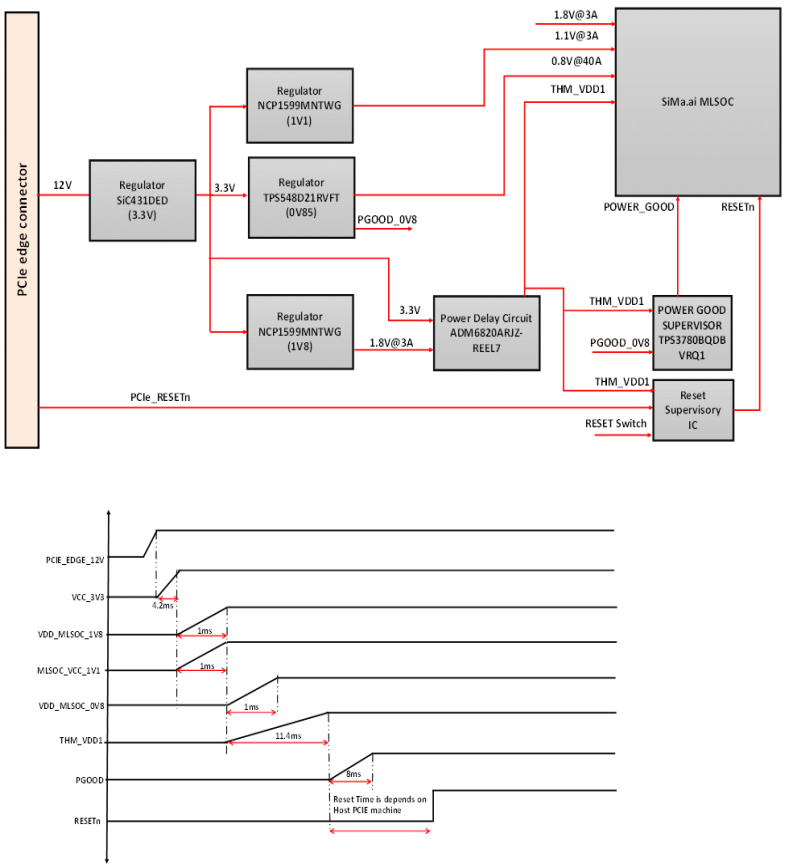

Figure 2-3. PCIe HHHL Board Power Up Sequencing Implementation

Figure 2-3. represents the preliminary implementation of the power sequencing of PCIe HHHL Board. The values which are given in “ms” are the soft-start time for each regulator. The current values in Amps are the maximum current which can be sourced by the regulator, not the actual power requirement. More details on power circuitry for entire board are provided in Chapter 4.

2.4 MLSoC Interfaces

This section contains detailed information about all the interface design enabled on the PCIe HHHL Board.

2.4.1 Single PCIe HHHL Board Specifications

Table 2-2. PCIe HHHL Board Specifications

Item	Name	Description
1	Processor/SoC	SiMa.ai MLSoC
2	LPDDR4	4 x 4GB SDRAM – LPDDR4
3	eMMC	16GB eMMC 5.1 industrial NAND
4	I^2C	2 x I^2C interface
5	1G Ethernet	2x 1G Ethernet with RJ-45 connector
6	UART	2 x UART interfaces
7	JTAG	1 JTAG
8	Quad SPI	1 x Quad SPI interfaces
9	PCIe Gen 4.0	PCIe Gen 4.0 x8 Interface
10	Cooling	Conduction/Air cooled
11	Operating Temperature	0°C to 70°C

2.4.2 LPDDR4 Interface (32-Bit)

- 4 x 32-bit LPDDR4 memory controllers are present in the MLSoC chip set.
- DRAM addressing up to 16GB is supported by the MLSoC.
- Each memory controller supports maximum of 933MHz clock frequency.
- Voltage requirement for each memory controller is as follows:
  - DDR_VDD = 0.85V
  - DDR_VDDQ = 1.1V
  - DDR_VAA = 1.8V
  - VREF voltage to be supplied internally.
- The ZN pin for connecting calibration resistor, of each memory controller must be pulled to ground through an external 120 ohms ±1% calibration resistor.

- ALERT_N signal is an output signal from the memory controller. So this signal of each controller needs to be connected to a test point on the board.
- 4 x 32-bit LPDDR4 chip sets with P/N MT53E1G32D2FW-046 IT:B from Micron should be mounted on the PCIe HHHL Board.
- Each LPDDR4 chip set is of 4GB density.
- Supporting four 32-bit LPDDR4 memory controllers and PHY interfaces operating at up to 3733 million transfers/s.
- Voltage requirement of each LPDDR4 IC is as follows,
  - VDD1 = 1.8V
  - VDD2 = 1.1V
  - VDDQ = 1.1V
- LPDDR4 chip set requires power sequencing. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ. Also, VDD1 must be greater than VDD2 and VDD2 must be greater than VDDQ – 200mV.
- Since separate controllers are present in MLSoC, command/address, control and data signals are connected one to one from MLSoC to LPDDR4 chip set.
- The ZQ calibration pins of DDR are connected to VDDQ through 240-ohm ±1% resistor.
- Zn and Zn_S pin of the MLSoC are shorted and connected to ground through 120-ohm ±1% resistor.
- LPDDR4 chip set command or address ODT control signals, ODT_CA_A, ODT_CA_B are pulled to VDD2 for enabling on-die termination.
- Power requirement for each memory controller in MLSoC is shown in **Table 2-3.**

Table 2-3. LPDDR4 Power Requirement Per Device

Item Number	Power Rail	Voltage (V)	Tolerance	Current Requirement (A)
1	VDD1	1.8	±100mV	0.033
2	VDD2	1.1	±40mV	1.012
3	VDDQ	1.1	±40mV	0.0105

Figure 2-4. shows the block level connection between MLSoC and LPDDR4

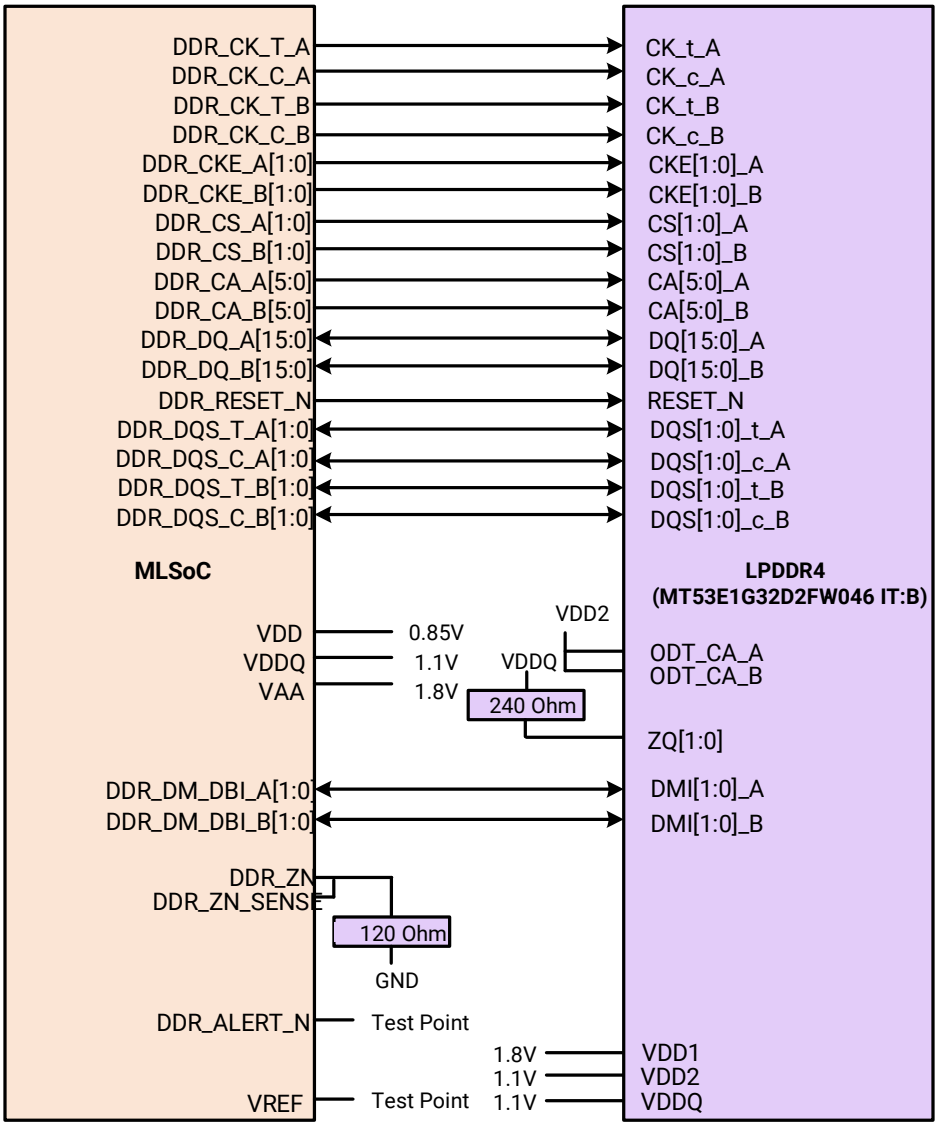

Figure 2-4. MLSoC to LPDDR4 Interface

MLSoC four DDR controller instances are connected to four LPDDR4 instances.

Table 2-4. LPDDR4 Interface Signal Pin-outs

Interface Signals		IO Description
MLSoC	**LPDDR4**	
DM_RST_N	RESET N	OUTPUT
DM_CSA[1:0]	CS[1:0]_A	OUTPUT
DM_CKEA[1:0]	CKE[1:0] A	OUTPUT
DM_CKTA	CK_t_A	OUTPUT
DM_CKCA	CK_c_A	OUTPUT
DM_CAA[5:0]	CA[5:0]_A	OUTPUT
DM_DQA[15:0]	DQ[15:0]_A	Bi-directional
DM_DMIA[1:0]	DMI[1:0]_A	Bi-directional
DM_DQSTA[1:0]	DQS[1:0]_t_A	Bi-directional
DM_DQSCA[1:0]	DQS[1:0]_c_A	Bi-directional
DM_CSB[1:0]	CS[1:0]_B	OUTPUT
DM_CKEB[1:0]	CKE[1:0]_B	OUTPUT
DM_CKTB	CK_t_B	OUTPUT
DM_CKCB	CK c_B	OUTPUT
DM_CAB[5:0]	CA[5:0]_B	OUTPUT
DM_DQB[15:0]	DQ[15:0]_A	Bi-directional
DM_DMIB[1:0]	DMI[1:0]_B	Bi-directional
DM_DQSTB[1:0]	DQS[1:0]_t_B	Bi-directional
DM_DQSCB[1:0]	DQS[1:0]_c_B	Bi-directional

2.4.3 MLSoC eMMC Interface

- eMMC controller in the MLSoC is compliant with eMMC 5.1 specifications and earlier versions.
- The MLSoC supports clock up to 52MHz.
- A 16GB eMMC flash with P/N SDINBDG4-16G-XI1 is used in PCIe HHHL Board.
- This is an eMMC 5.1 with HS400 interface eMMC flash (NAND type memory).
- The sequential read speed of this flash is 300MBps and the write speed is 80MBps.
- The voltage requirement for the eMMC flash IC is as follows:
  - Core Voltage (VC) = 3.3V
  - IO Voltage (VCCQ) = 1.8V

  See **Table 2-5.** for power requirements.
- The eMMC flash chip set supports variable clock frequencies of 0-20MHz, 0-26MHz (Default), 0-52MHz (high-speed), 0-200MHz SDR (HS200), 0-200MHz DDR (HS400).
- The PCIe HHHL Board detect pin EMMC_CRD_DET_N is pulled low to indicate that an eMMC flash is connected.
- eMMC write protect pin EMMC_CRD_WR_PROT is used to configure eMMC as read only. By default, this pin should be pulled high (write protected, read only).

Table 2-5. Power Requirement for eMMC Flash IC

Item Number	Power Rail	Voltage)	Tolerance	Current Requirement (A)
1	VCC	3.3	± 300mV	0.23
2	VCCQ	1.8	± 150mV	.295

Figure 2-5. represents the block level connection between the MLSoC and the eMMC flash.

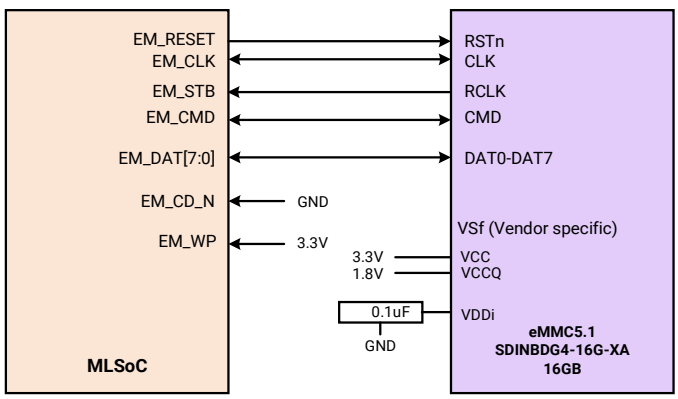

Figure 2-5. MLSoC eMMC Interface

See **Table 2-6.** for the MLSoC eMMC interface pin-out.

Table 2-6. MLSoC eMMC Interface Pin-out

Interface Signals		Signal Description
MLSoC	**eMMC**	
EMMC_CLK	CLK	OUTPUT
EMMC_CLK_FB	CLK	INPUT
EMMC_DAT_STB	EM_STB	INPUT
EMMC_CMD	CMD	Bi-directional
EMMC_RST_N	EM_RST	OUTPUT
EMMC_DAT[7:0]	DAT0-DAT7	Bi-directional
EMMC_CRD_DET_N (Card detect)	NA	INPUT
EMMC_CRD_WR_PROT (Write protect)	NA	INPUT

2.4.4 MLSoC I^2C Interface

- Two IC controllers are present in the MLSoC.
- I^2C controllers' clock frequency is up to 400 KHz for fast mode as per standard.
- All the I^2C SCL and SDA lines are provided by 2.2K-ohm pull-up resistors.
- I^2C0 and I^2C1 signals are connected to the 10-pin header and I^2C0 signal is connected to the PCIe edge connector as well.

Figure 2-6. shows the block level connection between the I^{2}C interfaces of the MLSoC.

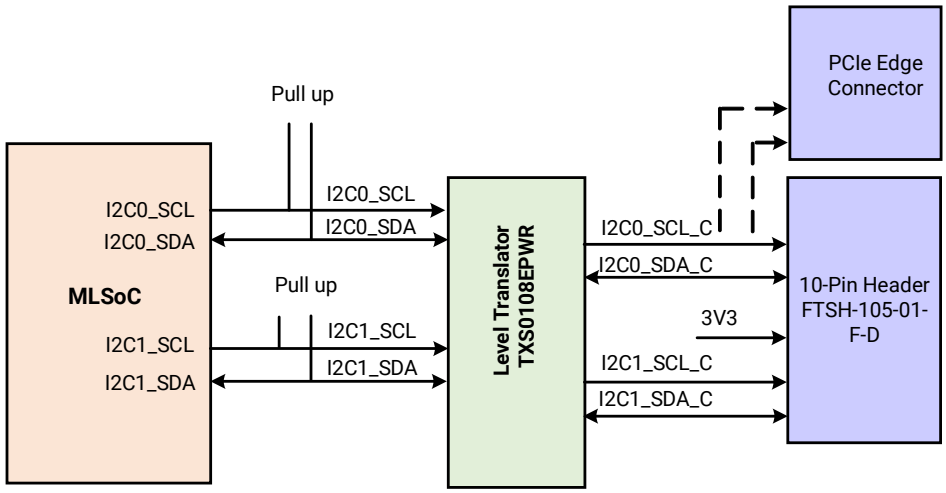

Figure 2-6. MLSoC I^{2}C Interface

Table 2-7. shows the PCIe HHHL Board pin-out.

Table 2-7. I^{2}C PCIe HHHL Board Pin-out

I^{2}C Interface Signal	Level Translator	I2C 10-pin Header Pin	PCIe Edge Connector Pin	IO Standards
I2C0_SCL	A1/B1	J1.5	J10.B5	Output
I2C0_SDA	A2/B2	J1.6	J10.B6	Bi-directional
I2C1_SCL	A3/B3	J1.1	X	Output
I2C1_SDA	A4/B4	J1.2	X	Bi-directional
3.3V power	NA	J1.9 & J1.10	X	Power
GND	NA	J1.3 & J1.7	X	Power
NC	NA	J1.4 & J1.8	X	No Connect

2.4.5 Ethernet Interface

- Four Gigabit Ethernet controllers are present in MLSoC chip set, but for PCIe HHHL Board only two Gigabit Ethernet interfaces are used.
- The MLSoC MAC supports 1000Base-KX or SGMII interface. In PCIe HHHL Board the SGMII interface from the MLSoC is directly brought out and connected to on-board Ethernet PHY.
- The voltage requirement for MLSoC Ethernet controller is as follows:
  - ETH_VP = 0.85V
  - ETH_VPH = 1.8V
- The Ethernet controller signals are differential pairs.
- 156.25MHz LVDS clock with P/N ASEMPLV-156.250MHZ-LR-T are connected to Ethernet controller reference clock pins.
- The Ethernet RESREF pin of controller for connecting reference resistor is connected with a 200-ohm ±1% resistor on the board.
- Voltage requirement for AR8031-AL1B is as follows,
  - VDD33 & AVDD33=3.3V.
  - VDDIO_REG & VDDH_REG = 2.5V Analog Supply
  - AVDDL2 & DVDDL= 1.1V Analog Supply
  - Ethernet PHY IC Interface signals are of 1.8V IO level.
- A 2.37k-ohm ±1% resistor is connected from RBIAS pin of PHY IC to GND
- SD pin of the PHY is tied to the DVDDL pin of the same IC with 10k-ohm resistor.

Table 2-8. describes the power requirements for the MLSoC Ethernet PHY.

Table 2-8. Power Requirements for MLSoC Ethernet PHY

Item Number	Power Rail	Voltage (V)	Tolerance	Current Requirement (A)
1	ETH_VPH	1.8	± 125mV	0.086
2	ETH_VP	0.85	± 110mV	0.05

Figure 2-7. shows the block diagram which represents the block level connections between the MLSoC and Ethernet.

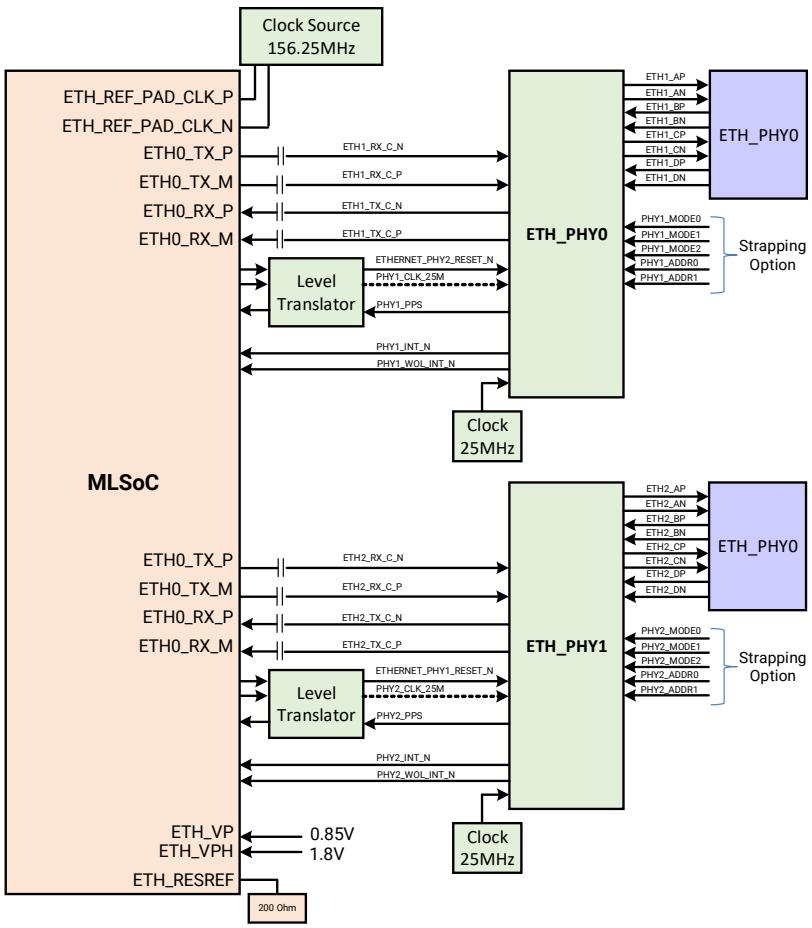

Figure 2-7. MLSoC Ethernet Interface

Table 2-9. shows Eth0 PHY mode and address configuration.

Table 2-9. Eth0 PHY Mode and Address Configuration

PHY Pin	PHY Core Config. Signal	Bit Configured in the Design	Description
RX_DV	PHY_MODE0	0	1000 BASE-T, SGMII
RXD2	PHY_MODE1	0	
RX_CLK	PHY_MODE2	0	
RXD3	PHY_MODE3	1	
RXD0	PHY_ADDR0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, “00”.
RXD1	PHY_ADDR1	0	
LED_ACT	PHY_ADDR2	0	

Table 2-10. shows the Eth1 PHY and address configuration.

Table 2-10. Eth1 PHY Mode and Address Configuration

PHY Pin	PHY Core Config. Signal	Bit Configured in the Design	Description
RX_DV	PHY_MODE0	0	1000 BASE-T, SGMII
RXD2	PHY_MODE1	0	
RX_CLK	PHY_MODE2	0	
RXD3	PHY_MODE3	1	
RXD0	PHY_ADDR0	1	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, “00”.
RXD1	PHY_ADDR1	0	
LED_ACT	PHY_ADDR2	1	

Table 2-11. shows the Ethernet Interface Pin-outs

Table 2-11. Ethernet Interface Pin-outs

Interface Signal MLSOC to PHY		IO Standards
MLSOC	**PHY IC**	
ETH_REF_PAD_CLK_P	ETH_REFCLK_156.250MHz_P	Ethernet REF clock +ve
ETH_REF_PAD_CLK_N	ETH_REFCLK_156.250MHz_N	Ethernet REF clock -ve
ETH0_TX_P	ETH1_TX_P	Ethernet1 Transmitter +ve
ETH0_TX_M	ETH1_TX_N	Ethernet1 Transmitter -ve
ETH0_RX_P	ETH1_RX_P	Ethernet1 Receiver +ve
ETH0_RX_M	ETH1_RX_N	Ethernet1 Receiver -ve
ETH1_TX_P	ETH2_TX_P	Ethernet2 Transmitter +ve
ETH1_TX_M	ETH2_TX_N	Ethernet2 Transmitter -ve
ETH1_RX_P	ETH2_RX_P	Ethernet2 Receiver +ve
ETH1_RX_M	ETH2_RX_N	Ethernet2 Receiver -ve
Interface Signals PHY to Magjack Connector		**IO Standards**
PHY IC	**Magjack**	
TRXP0	ETH1_AP	MDI0 +ve
TRXN0	ETH1_AN	MDI0 -ve
TRXP1	ETH1_BP	MDI1 +ve
TRXN1	ETH1_BN	MDI1 -ve
TRXP2	ETH1_CP	MDI2 +ve
TRXN2	ETH1_CN	MDI2 -ve
TRXP3	ETH1_DP	MDI3 +ve
TRXN3	ETH1_DN	MDI3 -ve

2.4.6 MLSoC UART Interfaces

- Five UART controllers are present in the MLSoC chip set. UARTB is used for Troot boot and UART2 is used for Linux boot function. The rest of the UARTs are not connected to any of the connectors.
- Level translators with P/N TXS0102DCT are used to convert MLSoC UART signals to 3.3 IO level.

Figure 2-8. shows the UART interfaces of the MLSoC.

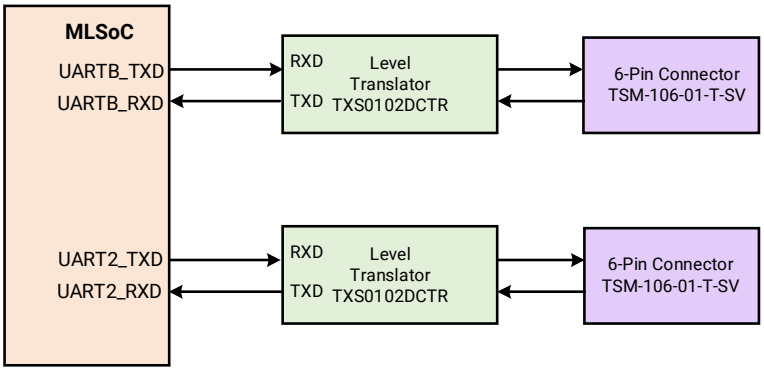

Figure 2-8. MLSoC UART Interface

Table 2-12. shows the UART interface pin-outs.

Table 2-12. UART Interface Pin-outs

Interface Signals		IO Standards
MLSoC	**Signal Name**	
UART_TX	TXD	OUTPUT, 3.3V
UART_RX	RXD	INPUT, 3.3V

Table 2-13. shows the UART connector pin-outs.

Table 2-13. UART Connector Pin-outs

6-pin Connector Pin		Signal Type
Pin No.	**Signal Name**	
1	GND	Ground
2	NC	Not Connected
3	NC	Not Connected
4	TXD	Transmit Asynchronous Data output
5	RXD	Receive Asynchronous Data input
6	NC	Not Connected

2.4.7 JTAG Interface

- One standard JTAG interface and one Test JTAG interface are present in the MLSoC. In PCIe HHHL Board, the Test JTAG connector is not populated.
- Normal JTAG interface is used for programming/debugging the MLSoC using an external programmer device.
- Since the MLSoC JTAG signal IO level is of 1.8V, JTAG buffer ICs with P/N SN74LVC244ARWP are used for the JTAG signals from the programmer device.
- One separate 14-pin connector with P/N: 15916142 is used for JTAG interface as well as the JTAG test signals interface.

Figure 2-9. shows a representation of both normal JTAG and Test JTAG interfaces of the MLSoC.

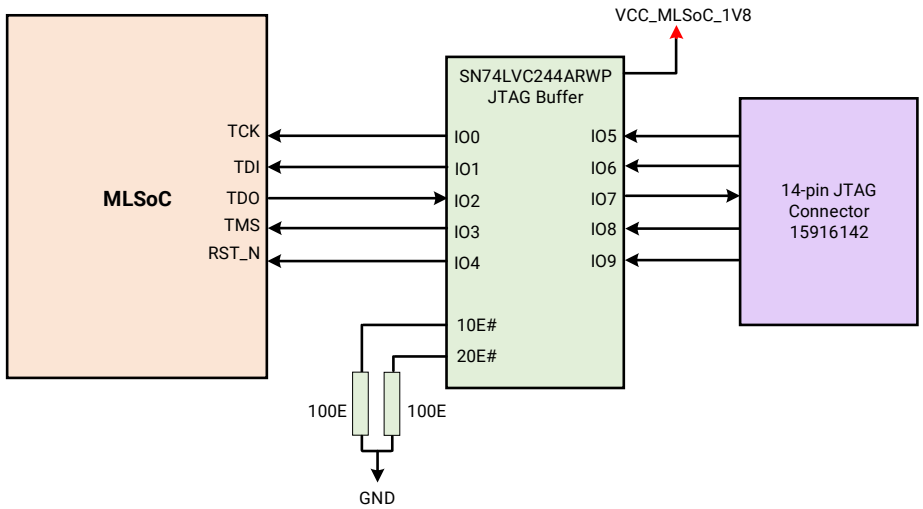

Figure 2-9. MLSoC JTAG Interface

Table 2-14. shows the MLSoC JTAG pin-outs.

Table 2-14. MLSoC JTAG Pin-outs

Signal Name	JTAG Buffer	IO Logic
TCK	1A2/1Y2	INPUT, 1.8V
TDI	1A3/1Y3	INPUT, 1.8V
TDO	2A1/2Y1	OUTPUT, 1.8V
TMS	1A1/1Y1	INPUT, 1.8V
RST_N	1A4/1Y4	OUTPUT, 1.8V

Table 2-15. shows the MLSoC JTAG connector pin-outs.

Table 2-15. MLSoC JTAG Connector Pin-outs

Pin Number	Signal Name	Description
5	VCC	Voltage
1	TMS	Test Mode Select
11	TCK	Test Clock
7	TDO	Test Data Out
3	TDI	Test Data In
2	TRSTn	RESET
8,10,12	GND	Ground
4,6,9,13,14	NC	No connect

2.4.8 MLSoC SPI-8 Interface

- One quad and two Octal SPI controllers are present in MLSoC chip set, namely SPIB, SPI0, and SPI1.
- SPIB controller from the MLSoC is used to connect the SPI Flash, where the initial boot loader is present and MLSoC boots after power on by reading this flash.
- In PCIe HHHL Board, both SPI_0 and SPI_1 controller signals are terminated as NC.
- A 128-Mbit Quad SPI Flash IC with P/N W25Q128JWSIQ is used as boot ROM. This IC is an 8-bit SPI with maximum clock rate of 133MHz.
- 10 POS 100Mils header connector with P/N 10129381-910004BLF is used for flashing the SPI through `Aardvark I2C/SPI Host Adapter`.

Figure 2-10. shows the MLSoC SPI-8 interface.

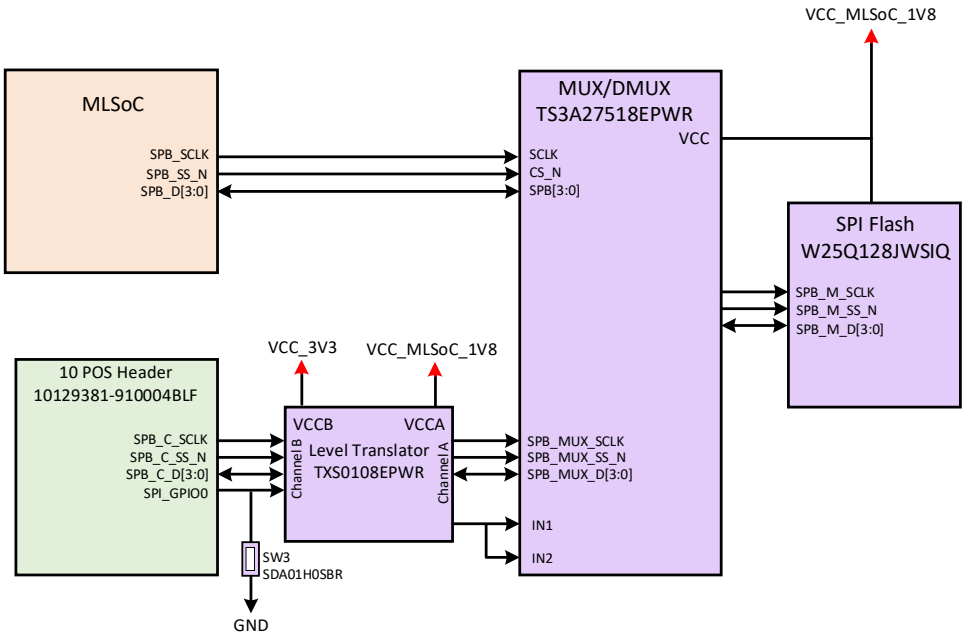

Figure 2-10. MLSoC SPI-8 Interface

Table 2-16. shows the MLSoC Quad SPI Flash Interface Pin-outs.

Table 2-16. MLSoC Quad SPI Programming Header Pin-outs

Pin Number	SPI Flash Signal Name	Description
J3.1	RESET_EXT	Externally controlled RESET Input
J3.3	SPI_GPIO0	GPIO to control MUX select line
J3.4	SPB_C_D2	SPI Data 2 Signal
J3.5	SPB_C_D1	SPI Data 1 Signal
J3.6	SPB_C_D3	SPI Data 3 Signal
J3.7	SPB_C_SCLK	SPI Clock Signal
J3.8	SPB_C_D0	SPI Data 0 Signal
J3.2, J3.9, J3.10	GND	Ground net

2.4.9 GPIO Interface

- 31 GPIO signals are present in MLSoC.
- Only 23 GPIOs are used in this design; the remaining GPIOs are NC.
- Each GPIOs connections are shown in **Figure 2-11.**

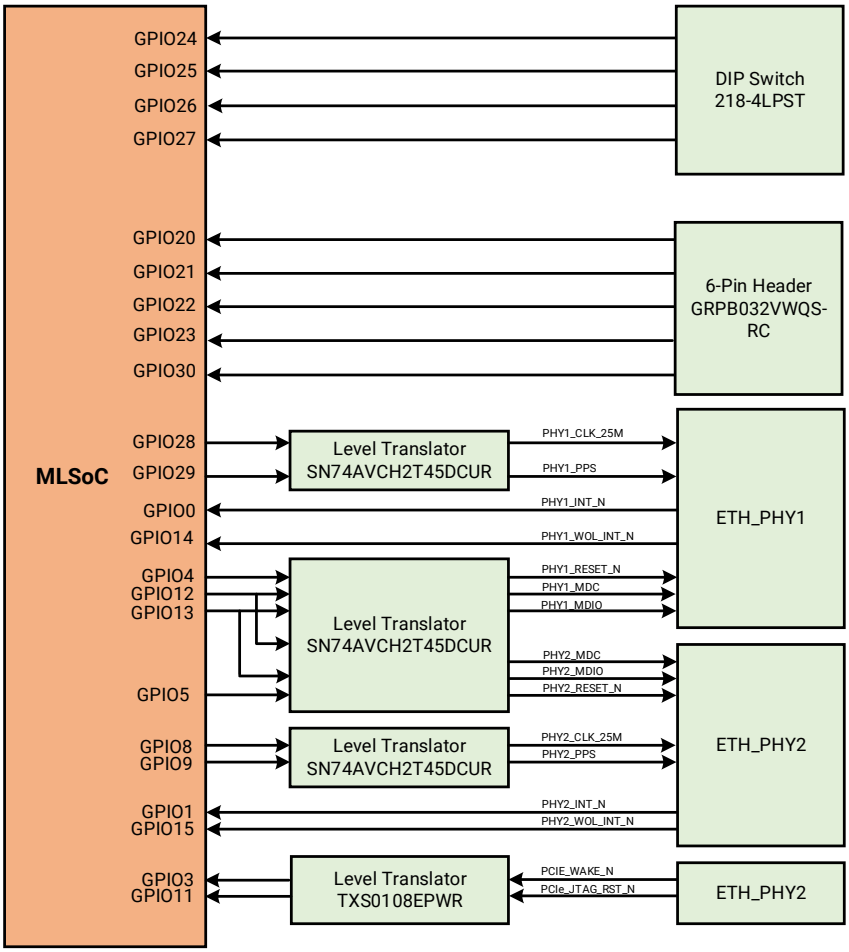

Figure 2-11. MLSoC GPIO Interface.

Table 2-17. shows the MLSoC GPIO Interface Pin-outs.

Table 2-17. MLSoC GPIO Interface Pin-outs

Pin Number	Signal Name in MLSOC	Description
U12.5	GPIO0	PHY1_INT_N
U22.5	GPIO1	PHY2_INT_N
J10.B11	GPIO3	PCIE_WAKE_N
U12.2	GPIO4	ETHERNET_PHY1_RESET_N
U22.2	GPIO5	ETHERNET_PHY2_RESET_N
U22.25	GPIO8	PHY2_CLK_25M
U22.22	GPIO9	PHY2_PPS

Table 2-17. MLSoC GPIO Interface Pin-outs (continued)

Pin Number	Signal Name in MLSOC	Description
J10.B9	GPIO11	PCIe_JTAG_RST_N
U12.1/U22.1	GPIO12	PHY1_MDC/ PHY2_MDC
U12.48/U22.48	GPIO13	PHY1_MDIO/ PHY2_MDIO
U12.40	GPIO14	PHY1_WOL_INT_N
U22.40	GPIO15	PHY2_WOL_INT_N
J2.1	GPIO20	General Purpose IO
J2.2	GPIO21	General Purpose IO
J2.3	GPIO22	General Purpose IO
J2.4	GPIO23	General Purpose IO
SW1.8	GPIO24	General Purpose IO
SW1.7	GPIO25	General Purpose IO
SW1.6	GPIO26	General Purpose IO
SW1.5	GPIO27	General Purpose IO
U12.25	GPIO28	PHY1_CLK_25M
U22.25	GPIO29	PHY2_CLK_25M
J2.5	GPIO30	General Purpose IO

2.4.10 PCIe Interface

- Hard PCIe Gen 4 x8 PHY controller is present in MLSoC chip set.
- Single PCIe Gen 4.0 lane supports link speed up to 16Gb/s.
- PCIe PHY supports only as endpoint during PCIE mode.
- On board 100MHz oscillator with P/N 510DBA100M000AAG is used as PCIe reference clock which is optional.
- The voltage requirement for PCIe PHY controller is as shown below.
  - PCIe_VP = 0.85V
  - PCIe VPH = 1.8V
- REFRES pin of PHY controller for calibrating the termination resistance of TX and RX lines is connected to a 200-ohm ±1% precision resistor.
- In PCIe HHHL Board all the PCIe lanes are connected to board edge connector and board operates only as an end point acceleration card.
- MLSOC that allows the physical lane ordering to be reversed between a device and the connector or target device.
- For ease of routing PCIE lane reversal is implemented during the routing.
- Standard two PCIe HHHL Board 98-pin board edge connections are used to interface the board with other boards.
- By default, the PCIe reference clock is from the ROOT PORT (Host side/motherboard) and not via on-board oscillator.

Figure 2-12. shows the x8 PCIe Gen 4 interface functional block diagram.

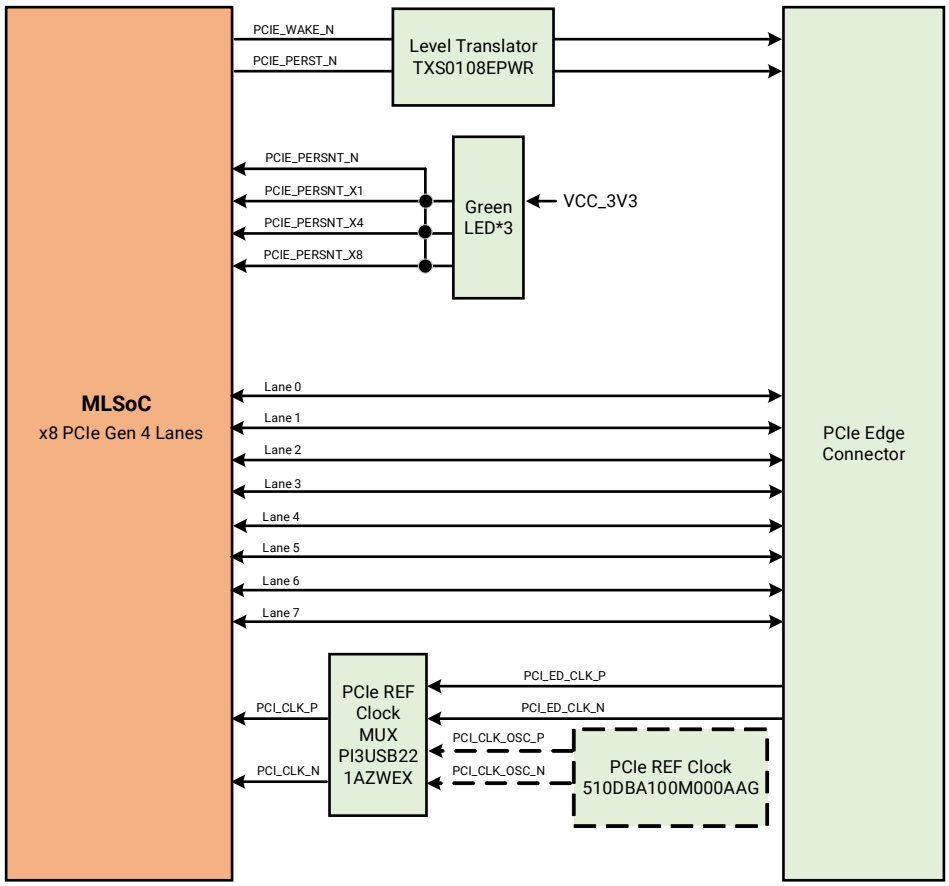

Figure 2-12. x8 PCIe Gen 4 Interface Functional Block Diagram

NOTE!

The only provision for on-board oscillator is given in the PCB. By default, this oscillator is not populated.

Table 2-18. shows the MLSoC PCIe Gen 4 x8 PCIe HHHL Board edge connector pin-outs.

Table 2-18. MLSoC PCIe Gen 4 x8 Dual PCIe HHHL Board Edge Connector Pin-outs

Edge Connector Pin Number	Edge Connector Signal Name	Signal Name	Description
J10.A12	PCIE_CLK_QO_C_P	PCI_ED_CLK_P	IN, PCIe Reference clock+
J10.A13	PCIE_CLK_QO_C_N	PCI_ED_CLK_N	IN, PCIe Reference clock-
J10.B14	PCIe_RX0_P	PCIE_RX_P[7]	IN, Lane 7 Receive Data+
J10.B15	PCIe_RX0_N	PCIE_RX_N[7]	IN, Lane 7 Receive Data-

Table 2-18. MLSoC PCIe Gen 4 x8 Dual PCIe HHHL Board Edge Connector Pin-outs

Edge Connector Pin Number	Edge Connector Signal Name	Signal Name	Description
J10.A16	PCIe_TX0_P	PCIE_TX_P[7]	OUT, Lane 7 Transmit Data+
J10.A17	PCIe_TX0_N	PCIE_TX_N[7]	OUT, Lane 7 Transmit Data-
J10.B19	PCIe_RX1_P	PCIE_RX_P[6]	IN, Lane 6 Receive Data+
J10.B20	PCIe_RX1_N	PCIE_RX_N[6]	IN, Lane 6 Receive Data-
J10.A21	PCIe_TX1_P	PCIE_TX_P[6]	OUT, Lane 6 Transmit Data+
J10.A22	PCIe_TX1_N	PCIE_TX_N[6]	OUT, Lane 6 Transmit Data-
J10.B23	PCIe_RX2_P	PCIE_RX_P[5]	IN, Lane 5 Receive Data+
J10.B24	PCIe_RX2_N	PCIE_RX_N[5]	IN, Lane 5 Receive Data-
J10.A25	PCIe_TX2_P	PCIE_TX_P[5]	OUT, Lane 5 Transmit Data+
J10.A26	PCIe_TX2_N	PCIE_TX_N[5]	OUT, Lane 5 Transmit Data-
J10.B28	PCIe_RX3_P	PCIE_RX_P[4]	IN, Lane 4 Receive Data+
J10.B29	PCIe_RX3_N	PCIE_RX_N[4]	IN, Lane 4 Receive Data-
J10.A29	PCIe_TX3_P	PCIE_TX_P[4]	OUT, Lane 4 Transmit Data+
J10.A30	PCIe_TX3_N	PCIE_TX_N[4]	OUT, Lane 4 Transmit Data-
J10.B33	PCIe_RX4_P	PCIE_RX_P[3]	IN, Lane 3 Receive Data+
J10.B34	PCIe_RX4_N	PCIE_RX_N[3]	IN, Lane 3 Receive Data-
J10.A35	PCIe_TX4_P	PCIE_TX_P[3]	OUT, Lane 3 Transmit Data+
J10.A36	PCIe_TX4_N	PCIE_TX_N[3]	OUT, Lane 3 Transmit Data-
J10.B37	PCIe_RX5_P	PCIE_RX_P[2]	IN, Lane 2 Receive Data+
J10.B38	PCIe_RX5_N	PCIE_RX_N[2]	IN, Lane 2 Receive Data-
J10.A38	PCIe_TX5_P	PCIE_TX_P[2]	OUT, Lane 2 Transmit Data+
J10.A39	PCIe_TX5_N	PCIE_TX_N[2]	OUT, Lane 2 Transmit Data-
J10.B41	PCIe_RX6_P	PCIE_RX_P[1]	IN, Lane 1 Receive Data+
J10.B42	PCIe_RX6_N	PCIE_RX_N[1]	IN, Lane 1 Receive Data-
J10.A42	PCIe_TX6_P	PCIE_TX_P[1]	OUT, Lane 1 Transmit Data+
J10.A43	PCIe_TX6_N	PCIE_TX_N[1]	OUT, Lane 1 Transmit Data-
J10.B45	PCIe_RX7_P	PCIE_RX_P[0]	IN, Lane 0 Receive Data+
J10.B46	PCIe_RX7_N	PCIE_RX_N[0]	IN, Lane 0 Receive Data-
J10.A47	PCIe_TX7_P	PCIE_TX_P[0]	OUT, Lane 0 Transmit Data+
J10.A48	PCIe_TX7_N	PCIE_TX_N[0]	OUT, Lane 0 Transmit Data-

Chapter 3
Clock Requirements

3.1 Clock Requirements

Table 3-1. describes the clock requirements on the PCIe HHHL Board.

Table 3-1. Clock Requirements

Item Number	Oscillator Frequency	Clock Source	Frequency Stability/Tolerance	Device	Interface
1	100MHz	Oscillator	±300ppm (or better)	MLSoC	PCIe PHY reference clock (optional interface).
2	33MHz	Oscillator	10ppm	MLSoC	Used as MLSoC reference clock
3	32.768KHz	Crystal	20ppm	MLSoC	RTC reference clock
4	156.25MHz	Oscillator	50ppm	MLSoC	Ethernet MAC Reference clock
5	25MHz	Crystal	25ppm	Ethernet physical IC	Reference clock for Ethernet Physical layer IC

Chapter 4
Power and Reset

This chapter describes the following topics:

- Power requirements
- Main Buck regulators for generating voltage 3.3V @ 24A
- Buck Regulator for MLSoC core voltage 0.85V @ 40A
- Buck regulator for LPDDR4 Controller VDDQ voltage and LPDDR4 IC 1.1V @ 3A
- Buck regulator for MLSoC IO voltages, LPDDR4 VDD, eMMC VDDQ 1.8 @ 3A
- System Reset

4.1 Power Requirements

The board has different power inputs for different configurations. During PCIe HHHL functionality, the board is powered through PCIe edge connector from the host computer or root complex. The main power input is connected to regulator circuitry to generate different power required for MLSoC and on-board interface circuitries. **Section 4.1.2** describes the entire board's power supply implementation details.

4.1.1 Circuit Protection

To suppress high-frequency noise thereby reducing the risk of equipment malfunction, the board includes EMI filters and ferrite beads, wherever necessary.

4.1.2 Power Tree

- All power supplies required for MLSoC and memory interfaces are generated from regulators separate from the regulators for generating the power supply for other interface circuitries on the board.
- 12V main supply is provided from the PCIe slot of the host machine. Three different Buck regulators are used for MLSoC power supplies as follows:
  - On-board Regulator for main supply 3.3V
  - Buck Regulator for Core Voltage 0.85V
  - Buck Regulator for IO voltage and LPDDR4 VDD1, eMMC VDD1 supply 1.8V
  - Buck Regulator for LPDDR4 and LPDDR4 Controller VDDQ Supply 1.1V
- IO voltage is ramped up before the core voltage of MLSoC.
- Different buck regulators and PMIC are used for power supply of other interfaces on the board.
- The 0.85V, 1.8V, and 1.1V are derived from 3.3V using a Regulator with P/N TPS548D21RVFT.

4.2 Main Buck Regulator for Generating 3.3V @ 24A

Part Number: SiC431DED

Package: PowerPAK MLP 44-24L

Operating Temperature: -40°C to +125°C

SiC431DED is a fully integrated buck converter with synchronous MOSFET switches and high-performance inductors. This IC will convert 12V to 3.3V@24A and is used for supply the power to all the regulators. A wide range of input from 3V to 24V can be supplied to this IC.

Visit this link for details.

4.3 Buck Regulator for MLSoC Core Voltage 0.85V @ 40A

Part Number: TPS548D21RVFT

Package: LQFN-CLIP

Operating Temperature: -40°C to +125°C

TPS548D21RVFT is a fully integrated buck converter with synchronous MOSFET switches and high performance inductors. This IC will convert 3.3V to 0.85V@40A and is used for power-supply pins for the internal core logic of the MLSOC. A wide range of input from 1.5V to 16V can be supplied to this IC. Since IO voltage of MLSoC shall ramped up before the core voltage, the CTRL pin of this IC shall be connected to IO voltage regulator output.

Visit this link for details.

4.4 Buck Regulator for LPDDR4 Controller VDDQ Voltage and LPDDR4 IC 1.1V @ 3A

Part Number: NCP1599MNTWG Package: DFN6

Operating Temperature: -40°C to +85°C

This buck regulator is used to generate 1.1V@3A from the 3.3V regulated supply and is supplied to MLSoC LPDDR4 VDD2, VDDQ and LPDDR4 Controller VDDQ Pins. This IC comes with integrated MOSFETs and Inductor. Also has wide input range from 3V to 5.5V.

Visit this link for details.

4.5 Buck Regulator for MLSoC IO Voltages, LPDDR4 VDD, eMMC VDDQ 1.8 @ 3A

Part Number: NCP1599MNTWG Package: DFN6

Operating Temperature: -40°C to +85°C

This buck regulator is used to generate 1.8V@3A from the 3.3V regulated supply. The output voltage is supplied for MLSoC IO voltage, LPDDR4 VDD1 and other voltages required for different interface controllers. This IC comes with integrated MOSFETs and Inductor. Also has wide input range from 3V to 5.5V.

Visit this link for details.

4.6 Reset

Power ON reset functionality of MLSoC is implemented by asserting PERST# and can also be used by the system to force a hardware reset button on the board.

NOTE!

Board Power up is completed and it comes out of reset. Once the chip is out of reset, then MLSoC should boot and PHY settings need to be applied to the PCIe PHY before the PERST# de-asserts. **Figure 4-13.** shows the system reset.

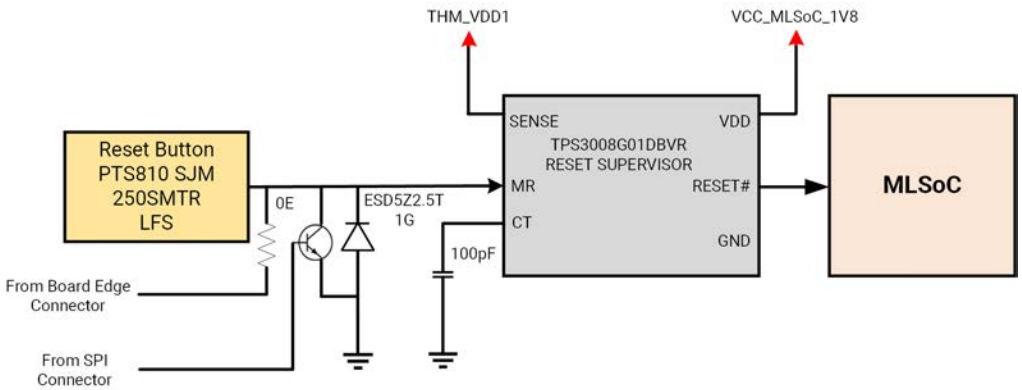

Figure 4-13. System Reset

- On-board reset switch with P/N PTS810 SJM 250 SMTR LFS is used to reset the board.
- An ESD protection diode with P/N ESD5Z2.5T1G is used to protect MLSoC from high surges.
- The capacitor in the CT pin is used to select the RESET delay time manually.

Chapter 5
Operation and Maintenance

This chapter describes the following topics:

- LED features
- Test points

5.1 LED Features

The LED features as shown in **Table 5-1.** are supported on the PCIe PHHHL Card.

Table 5-1. LED Requirements

Item Number	Signal	LED Color	Status
1	RESET_IN_N	RED	MLSOC reset
2	PCIE_PRSNT_N_X1	GREEN	X1 PCIe present
3	PCIE_PRSNT_N_X4	GREEN	X4 PCIe present
4	PCIE_PRSNT_N_X8	GREEN	X8 PCIe present

5.2 Test Points

Depending on the space availability, test points are provided (wherever necessary) for voltages and ground.

Chapter 6
PCB and Packaging

This chapter describes the following topics:

- PCB size and thickness
- Board layer description

6.1 PCB Dimensions

- PCB size (standard PCIe HHHL Board form factor): 160mm (L) × 68.9mm (H)
- PCB thickness: 1.6mm (H)

6.2 Board Layer Description

The PCB stack-up includes 12 layers and the layer sequence is as shown in **Table 6-1.**

Table 6-1. PCB 12 Layer Stack-up

Item Number	Layer Description
1	TOP
2	GND1
3	SIG1
4	GND2
5	SIG2
6	VCC1
7	VCC2
8	SIG3
9	GND3
10	SIG4
11	GND4
12	BOTTOM

Chapter 7
Signal and Power Integrity Analysis

This chapter describes the following topics:

- Pre-layout Signal Integrity (SI) Analysis
- Post-layout Signal Integrity Analysis
- Power Integrity (PI) Analysis
- Thermal Analysis

Signal and power integrity are the major factors which decide the performance and functionality of a device. The analyses for the for PCIe, ETH, and DDR during the layout design stage of MLSoC stage are described in this chapter.

7.1 Pre-layout SI Analysis

Pre-layout SI Analysis are done once the placement is finalized and before starting the routing of the signals. The main purpose of the pre-layout analysis is to develop design constraints.

7.2 Post Layout SI Analysis

Post Layout SI Analysis is done after the layout design and feedback is implemented. The following are the major analyses which are carried out for ETH, PCIe, and DDR interfaces. The Post Layout SI analysis verifies the compliance to the design constraints.

S parameter Analysis (Insertion loss, Return Loss, FEXT & NEXT): The S-parameter simulation is a well-suited tool to characterize the complex circuits at high frequency to ensure its signal integrity. S-parameter simulation is one type of AC simulation that presents the small signal behavior of the device at the given temperature, bias conditions, and input signals.

- *Crosstalk Analysis*: Cross talk occurs when energy in one signal couples onto another signal. To avoid this, signal spacing, voltage swing, distance to ground, typical cross talk, and typical route length are analyzed.
- *Eye Analysis*: Eye diagrams helps to identify the signal quality and the noise margins. This helps in identifying the noise sources and in improving the signal quality.

7.3 PI Analysis

Post-layout PI Analysis is done after the layout design and feedback is implemented. The following is the major analysis carried out:

- IR- Drop Analysis: There are many interdependent factors that can impact IR drop including signal flow path, trace geometry, thermal effect, impedance matching, and count and size of via.

7.4 Thermal Analysis

Board level thermal analysis is done for ambient temperature and feedback is implemented. This help in identifying temperature dense areas on the board for ambient temperature. The thermal analysis result is considered for heat sink design for the MLSoC by SiMa.ai.

Chapter 8
Certification Data

The EUT was configured for testing in accordance with requirements of the EN 55032: 2015/A11: 2020, BS EN 55032:2015+A1:2020, and EN/BS EN 55035:2017/A11:2020 standards.

This chapter provides certification data and describes the summary of test results.

8.1 Summary of Test Results

8.1.1 Emissions

Table 8-1. shows the Emissions results.

Table 8-1. Emissions

Standard	Test Description	Result
EN/BS EN 55032 Section A.3	Conducted Emissions	Note[a]
EN/BS EN 55032 Section A.2	Radiated Emissions	Compliant with Class A Limits
EN/BS EN 61000-3-2	Harmonic Current Emissions	Note[a]
EN/BS EN 61000-3-3	Voltage Fluctuation and Flickers	Note[a]

a. The EUT was DC powered.

NOTE! Signal Line/Data cables were not longer than 3m in length.

Table 8-2. shows the Immunity results.

Table 8-2. Immunity Results

Standard	Test Description	Result
EN/BS EN 55035 Section 4.2.1	Electrostatic Discharges EN/BS EN 61000-4-2	Compliant
EN/BS EN 55035 Section 4.2.2.2	Continuous Radiated Disturbances EN/BS EN 61000-4-3	Compliant
EN/BS EN 55035 Section 4.2.4	Electrical Fast Transients EN/BS EN 61000-4-4	Note[a]
EN/BS EN 55035 Section 4.2.5	Surges EN/BS EN 61000-4-5	Note[a]
EN/BS EN 55035 Section 4.2.2.3	Continuous Conducted Disturbances EN/BS EN 61000-4-6	Note[a]
EN/BS EN 55035 Section 4.2.3	Power-frequency Magnetic Fields EN/BS EN 61000-4-8	Compliant
EN/BS EN 55035 Section 4.2.6	Voltage Dips and Interruptions EN/BS EN 61000-4-11	Note[a]

a. The EUT was DC powered.

NOTE!

Signal Line/Data cables were not longer than 3m in length.

A complete Certification report (*SiMa R2301133-2- Final.pdf*) is available from SiMa.ai. Please contact SiMa.ai to get a copy of this report.

Chapter 9
Environmental and Compliance Specifications

This chapter describes the following topics:

- Environmental requirements
- Environmental specifications
- EMI/EMC and other compliance

9.1 Environmental Requirements

The operating temperature range of the PCIe HHHL Board is 0° C to 70° C (commercial grade).

9.2 Environmental Specifications

Cooling Method: Conduction/air cooled

9.3 EMI/EMC and Other Compliance

The EMI/EMC (Electromagnetic Interference/Electromagnetic Compatibility) design guidelines need to be followed as per the device's datasheet. Also follow the general PCB design guidelines to avoid the EMI/EMC-related issues.

Follow these precautions during the design:

1. Try to use Switching Regulator with integrated/built in inductor.
2. Use EMI/EMC common mode filter and power filters at the entrance of the power.
3. Power plane routing should not be zigzag. Power plane needs to be straight from the source to the sink.
4. All the power must have an immediate ground reference.

Chapter 10
Support

If you have questions, please contact our support team in one of two ways:

- Submit your request at https://simaai.zendesk.com
- Email: support@sima.ai

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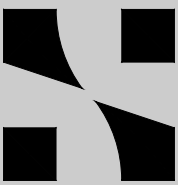

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