SM1 Datasheet

Document No: 001-HW-24, Rev. D

June 24, 2024

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Revision History

Date	Version	Description
September 30, 2022	A	• Initial release.
November 15, 2022	B	• Made minor change in See "General-Purpose I/O" on page 20. • Updated "Power-Up and Reset Timing" on page 23. • Added Table 5-2, "MLSoC SM1 Pin and Signal Names," on page 45. • Added Table 6-1, "Nominal Voltages, Power Supplies, and Tolerance Ranges," on page 69. • Updated Table 7-1, "MLSoC Package Dimensions," on page 75
June 9, 2023	C	• Updated "Reference Documentation" on page 11 and added Developer Zone website information for SiMa.ai customers. • Updated "General-Purpose I/O" on page 20. • Removed old Chapter 6 MLSoC Reliability and Qualification Information and reorganized the rest of the book. • Added Table 8-1, "Commercial and Industrial Grade Operating Range," on page 77 in Chapter 7 "MLSoC Ordering Information" on page 73.
June 24, 2024	D	• Updated voltage and power supply tolerance range information for VDD in Table 6-1 on page 69. • Added the section on "Recommended Power Supply Distribution" on page 24.

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About this Document

The Machine Learning System on Chip (MLSoC™) from SiMa.ai delivers high-performance, effortless machine learning inference for embedded edge applications. Built on 16nm technology, the MLSoC's processing system consists of computer vision processors for image pre-processing, coupled with dedicated machine learning acceleration and high-performance application processors. Surrounding the real-time intelligent video processing are memory interfaces, communication interfaces, and system management all connected via a network on chip (NoC).

The SiMa.ai MLA IP is the core of the SiMa.ai MLSoC which provides a platform for accelerating next generation machine learning applications.

Purpose and Scope

This document provides the necessary information related to the MLSoC SM1 that is needed to incorporate this product into the customer application. It covers the following topics:

- Overview
- Functional Modules
- Power management and electrical specifications
- Pinout and signal description
- MLSoC reliability and qualification information
- MLSoC packaging information
- MLSoC ordering information
- Support

Intended Audience

This document is intended for HW/ML engineers who are interested in deploying SiMa.ai MLSoC into their designs. An advanced knowledge of Arm-based processing systems, computer vision, memory interfaces, video processing, and machine learning networks for the intended application is required. It is assumed that the user is familiar with SiMa.ai Machine Learning Accelerator (MLA), Linux fundamentals, and Python.

Reference Documentation

These documents provide additional information in understanding the SiMA.ai MLSoC and SDK.

Document Name	Description
SiMa.ai Documents	
Machine Learning System on Chip (MLSoC™) Product Brief	Provides MLSoC highlights, overview and architecture features.
MLSoC™ Developer Board Product Brief	Describes key features of the MLSoC. In addition, it provides a functional block diagram that shows all the major blocks of the Evaluation Platform.

Document Name	Description
Ethernet Boot of MLSoC™ Evaluation Board	Describes how to install the Ethernet boot process of the SiMa.ai MLSoC Evaluation Board in order to run the customer pipeline.
MLSoC™ Board User Guide	Describes how to configure and use the MLSoC Evaluation Board.

Internal/External URL Links for Additional Documents	Description
1. https://developer.sima.ai/	Developer Zone for SiMa.ai customers. Request access for the latest software download and documentation by sending email to: developer.mlsoc@sima.ai

Chapter 1
Overview

This chapter provides an overview of the MLSoC SM1.

SiMa.ai MLSoC delivers high-performance, effortless machine learning for embedded edge applications. Built on 16nm technology, the MLSoC's processing system consists of computer vision processors for image pre-processing, coupled with dedicated machine learning acceleration and high-performance application processors. Surrounding the real-time intelligent video processing are memory interfaces, communication interfaces, and system management all connected via a network on chip (NoC).

The MLSoC features low operating power and high ML processing capacity, making it ideal as a standalone edge-based system controller, or to add a machine learning offload accelerator for processors, ASICs, and other devices.

1.1 MLSoC SM1 Functional Blocks

The MLSoC contains the following major functional blocks:

- **Machine learning accelerator (MLA)** – providing up to 50 teraoperations per second (50 TOPS) for neural network computation.
- **Application processing unit (APU)** – a cluster of four ARM Cortex-A65 dual threaded processors operating up to 1.15 GHz to deliver up to 15K Dhrystone MIPs.
- **Video encoder/decoder** – supports the H.264 compression standards HEVC (High Efficiency Video Coding) with support for baseline/main/high profiles, 4:2:0 pixels and 8-bit precision. The decoder also supports H.265 baseline/main/high profiles. The encoder supports rates up to 4K P30, while the decoder supports up to 4K P60.
- **Computer vision unit (CVU)** – consists of a four-core Synopsys ARC EV74 video processor supporting up to 600 16-bit GOPS.
- **High-speed I/O subsystem** – provides four 1 Gigabit Ethernet ports plus a PCIe Gen4 8-lane interface as an endpoint.
- **Low-speed I/O subsystem** – lower bandwidth interfaces such as SPI, I^2C, GPIO, and SDIO/eMMC flash interfaces.
- **DRAM interface system (DIS)** – supporting four 32-bit LPDDR4 memory controllers and PHY interfaces operating at up to 3733 MTps.
- **Boot and security unit (BSU)** – provides secure key storage in non-volatile memory (efuse) and key management. Supports decryption and authentication of the boot image as well as providing a security API to the user code.

See **"Figure 1-1."** for details.

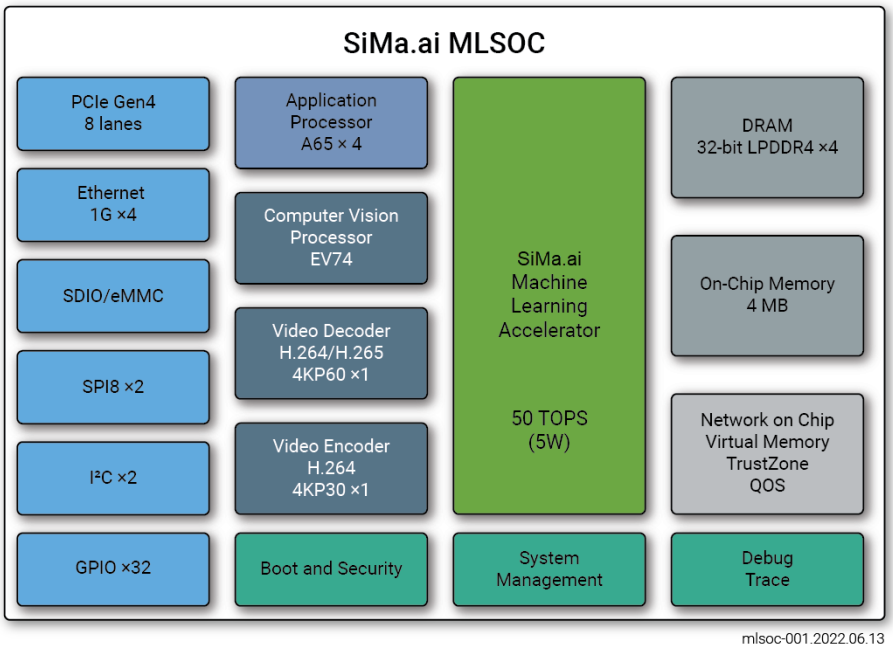


Figure 1-1. MLSoC Block Diagram

Chapter 2
MLSoC SM1 Functional Modules

The MLSoC delivers high-performance, effortless machine learning inference for embedded edge applications, containing the following major functional blocks:

- Machine learning accelerator (MLA)
- Application processing unit (APU)
- Video encoder/decoder
- Computer vision unit (CVU)
- MLSoC Interfaces
- DRAM interface system (DIS)
- Boot and security unit (BSU)

2.1 Machine Learning Accelerator

The machine learning accelerator (MLA) is a high-performance (up to 50 TOPS), low-power, instruction-based accelerator for machine learning applications operating on tensors. The MLA's program is compiled from neural network descriptions in TensorFlow and other graph-based neural-network formats.

The embedded MLA is constructed from a 10 × 10 array (mosaic) of computational tiles, each of which provides 256 8-bit MACs together with a 16-element, 32-bit element-wise processor and interpolated look-up tables. The MLA can also be divided into four quads of 25 tiles or two halves of 50 tiles, each working independently.

Overall block specifications:

- Up to 51.2 trillion 8-bit operations per second
- Four DMA engines for input/output data, weights
- Each of the four DMA engines has a built-in decompression (DCMP) engine
- A separate DMA engine for instructions
- AXI-based interfaces for data transfer
- APB-based interface for registers accesses
- Integrated Arm Cortex-M4 processor for managing MLA functionality

See "Figure 2-1." below.

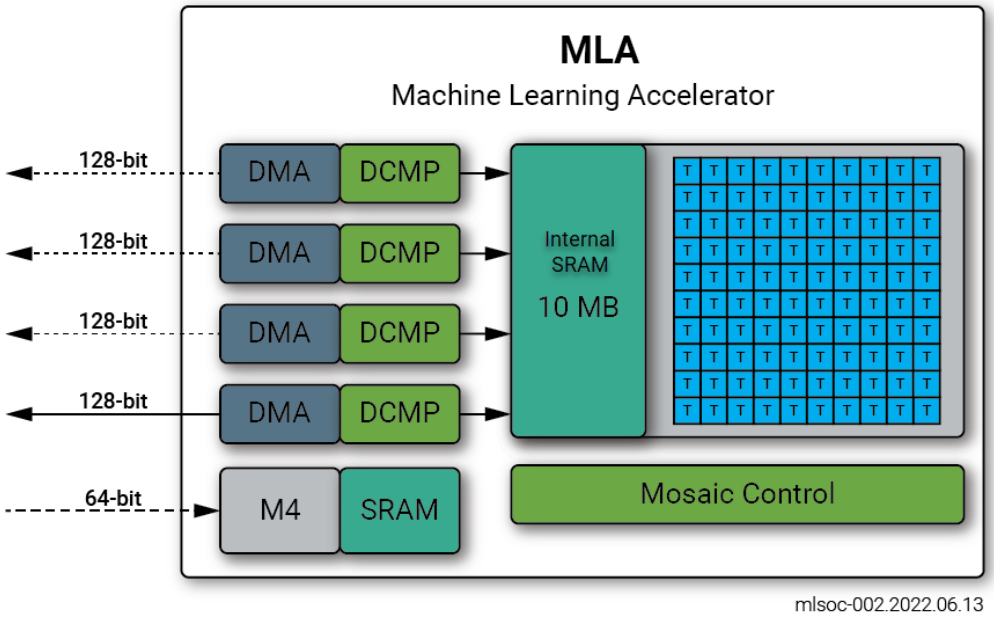


Figure 2-1. MLA Block Diagram

2.2 Application Processing Unit

The application processing unit (APU) that runs user application code, is composed of a cluster of four Arm Cortex-A65 dual threaded processors operating at up to 1.15 GHz to deliver up to 15 kilo-Dhrystone (KD) MIPs.

The processors are organized into a DynamicIQ cluster along with a DynamicIQ shared unit (DSU). The DSU itself consists of a level-three (L3) memory system, control logic, and external interfaces to support a DynamIQ cluster.

Each Cortex-A65 core supports two threads simultaneously and contains the Arm advanced single instruction, multiple data (SIMD) extension (NEON) to achieve superior performance. The associated NEON units provide an additional 16 GOPS of 16-bit integer operations.

Each core has an L1 cache (composed of a 32-KB I-cache and a 32-KB D-cache) plus an associated 128-KB L2 cache. All four cores share 1MB of L3 cache.

Core features:

- Full implementation of the Armv8.2-A A64 instruction set
- AArch64 execution state at all Exception levels (EL0 to EL3)
- Superscalar, variable-length, out-of-order pipeline
- Simultaneous multithreading, with two execution threads on each core
- Memory management unit (MMU)
- Support for Arm TrustZone technology

2.3 Video Encoder

The MLSoC video encoder is used to compress video data for archiving or remote inspection. It is possible to selectively compress just the video frames of interest. The embedded video encoder supports an aggregate throughput of 30 4K frames per second.

Supported video modes:

- Up to 4K p30
- H.264 High/Main/Baseline
- 8-bit
- 4:2:0

2.4 Video Decoder

A typical machine learning system may include remote cameras to send compressed video streams over Ethernet or PCIe to the MLSoC. The embedded video decoder supports an aggregate throughput of 60 4K frames per second.

Supported video modes:

- Up to 4K p60
- H.264/H.265 High/Main/Baseline
- 8-bit
- 4:2:0

2.4.1 Video Camera Streams Support

A maximum of eight camera streams are supported. "Table 2-1." shows the number of video camera streams supported with different resolutions and frames per second.

Table 2-1. Video Camera Streams Supported

Number of Camera Streams	Resolution/Frame Per Second
8	1080p @30fps
4	1080p @60fps
4	2K @30fps
2	2K @60fps
2	4K @30fps
1	4K @60fps

2.5 Computer Vision Unit

The computer vision unit (CVU) consists of a four-core Synopsys ARC EV74 video processor supporting up to 600 16-bit GOP/s running at 800 MHz. These cores are derived from the ARC HS family of processors, and is a combination of a high-performance ARC scalar core and an ARCv2 Vector DSP unit for single-instruction multiple-data (SIMD) processing. The CVU consists of the following major blocks:

- CVU processor core – the main processing unit of the CVU consisting of a scalar CPU, a vector DSP, and associated memory caches.
- Streaming transfer unit (STU) – used to transfer data from system memory to the internal memories in the CVU.
- Cluster shared memory (CSM) – provides a high-capacity, high-throughput memory shared by all cores within the CVU.
- ARConnect – block acts as a cluster controller and supports timer and IRQ management, inter-process messaging, power management and debug facilities. The ARConnect block is accessible via the AXI slave interface.
- CVU Interfaces – supports an I/O coherent a quad AXI interface for DMA into or out of the CVU. A 128-bit AXI master interface allows the CVU cores to access system memory. The CSM has a 128-bit DMI allowing other on-chip DMA controllers to transfer data directly into the CSM.

See **"Figure 2-2."** for details.

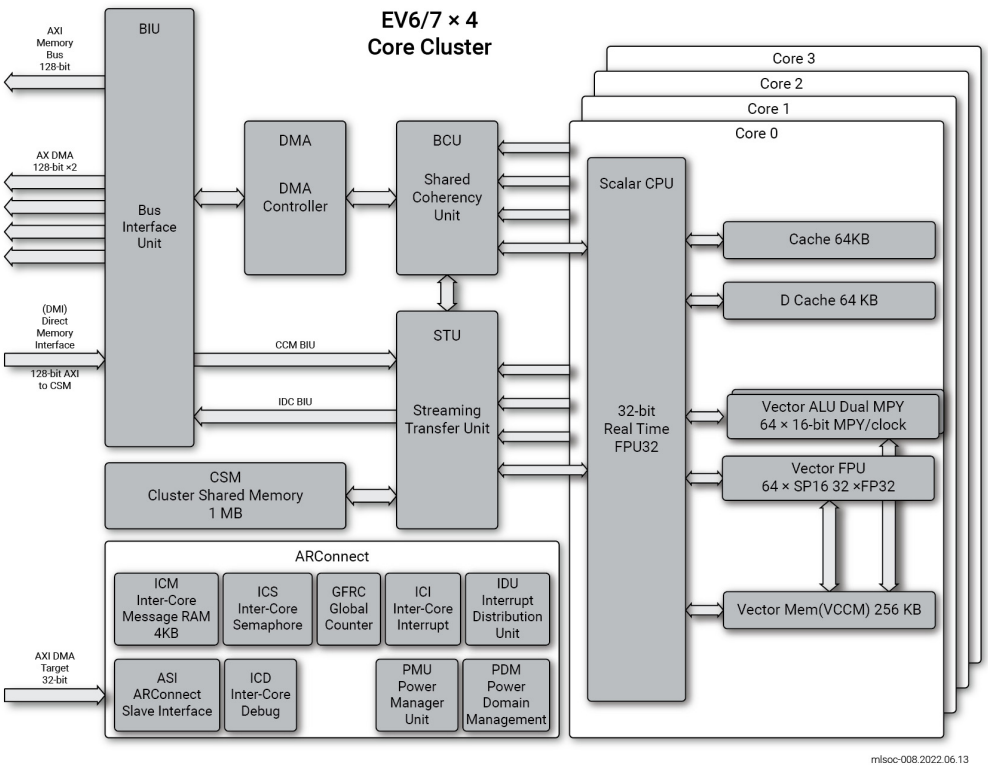


Figure 2-2. CVU Block Diagram

2.6 MLSoC Interfaces

2.6.1 High-Speed Interfaces

2.6.1.1 PCIe Gen4

Each MLSoC includes an embedded PCIe 8-lane Gen4 interface. The MLSoC can only be a single EP.

2.6.1.2 1G Ethernet

The MLSoC supports four 1 Gbps SGMII Ethernet ports.

The MLSoC GigE subsystem supports the following:

- Four independent, one Gbps Ethernet lanes
- 802.3-2018 compliant (1000-BASE-KX). An external PHY is needed to enable 1000-BASE-T connectivity.
- Support for 1GE
- Support for Jumbo Frames

2.6.2 Low-Speed Interfaces

2.6.2.1 eMMC Flash Memory Interface

The eMMC controller in the MLSoC is designed to provide rapid access to external flash memory device operating at 50MHz. External flash memory can be used to store boot code, operating system, application code, and data. The controller is compliant with eMMC 5.1 specifications and earlier versions. For machine learning applications, weights can also be stored in external flash memory and transferred to DRAM before use.

2.6.2.2 SDIO Flash Memory Interface

The SDIO controllers in the MLSoC are designed to provide rapid access to external flash memory devices operating at 100MHz. External flash memory can be used to store boot code, operating system, application code, and data. The controller is compliant with the SD 6.0 and SDIO 4.10 specifications and earlier versions. For machine learning applications, weights can also be stored in external flash memory and transferred to DRAM before use.

2.6.2.3 Serial Peripheral Interface

Serial peripheral interface (SPI) allows synchronous serial communication (full duplex or half duplex) with continuous streaming of data communicated between the controller and one or more peripheral devices. The dual embedded SPI controllers allow the MLSoC to communicate with external sensors, ADCs, flash memory, and other low data-rate peripherals.

Each of the MLSoC SPI interfaces features:

- 8-bit operation
- Four slave selects
- Dual master/slave mode
- 25 MHz SDR operation
- Supports quad and octal SPI flash devices

2.6.2.4 I^2C Interface

I^2C is a low-speed, two-wire interface operating at data rates of up to 1 Mbps. The MLSoC features two I^2C interfaces for connecting to low-bandwidth peripherals.

2.6.2.5 UART

MLSoC provides four general-purpose RS-232-compliant interfaces for communicating with legacy systems. For standard baud rates, the UART supports operation up to 3.68 MBaud.

There is a fifth UART dedicated to the BSU. Refer to **"2.8. Boot and Security Unit"** for details.

2.6.3 General-Purpose I/O

Each MLSoC features up to 32 independently programmable general-purpose I/O (GPIO) to control various external pins. Each I/O pin can be set individually by the processor, or the processor can read back the GPIO state. GPIO 0 - 7 can be used for interrupting the APU.

The MLSoC GPIO features CMOS drivers with tri-state support.

2.6.4 JTAG

The MLSoC supports one IEEE 1149.1 compliant JTAG port for A65 or EV74 debug.

2.7 DRAM Interface System

The MLSoC uses off-chip LPDDR4 DRAM to store application code, operating system code as temporary storage for machine learning data being processed.

To support this off-chip storage, the MLSoC includes a high-performance DRAM controller specifically optimized for storing the weights associated with machine learning algorithms. Weights stored in off-chip DRAM are streamed through the MLA along with each image frame to produce the resulting data.

DRAM controller features:

- Support for LPDDR4 32-bit, up to 3733 MTps
- Four 32-bit interfaces are supported
- Max density of 4 GB per interface
- Single or double rank for multi-die package support
- RAS support
  - Inline ECC

2.8 Boot and Security Unit

The boot and security unit (BSU) manages all the security and boot functions within the MLSoC, and is powered by an embedded security processor — a Synopsys 32-bit EM4 microprocessor. The security processor has access to 128 KB of internal SRAM, organized as an Instruction Closely Coupled Memory (ICCM) and Data Closely Coupled Memory (DCCM), each 64 KB in size. BSU supports an RTC, an UART, and a dedicated boot SPI interface.

The security system has two primary functions:

- Upon the deassertion of Reset, the BSU boots the device in a secure manner, establishing a root of trust based on the keys stored in BSU's eFuse. MLSoC supports up to eight customer keys.
- After the device is operating, the BSU provides encryption and decryption services through a software API and manages the cryptographic keys.

2.8.1 Boot SPI

The SPI Flash used for the Boot SPI interface has to be quad-enabled. This SPI interface is dedicated for boot and is separate from the two generic SPI interfaces.

2.9 System Management

2.9.1 Clock and Reset Unit

The clock and reset unit allows the software to enable clocks and reset specific blocks of the chip. It covers the following clocks:

- APU
- MLA
- CVU
- DDR
- PCIe
- Ethernet
- VID
- eMMC
- SDIO
- SPI
- I2C

Software can control all the PLLs on the chip.

2.9.2 Thermal Monitor

The MLSoC has an on-chip thermal monitor that can be used to measure the die temperature. The software has the ability to measure the temperature in the key areas of the chip using these monitors. The temperature measured using the thermal monitor is within ±3% accuracy if used in conjunction with the calibration values already stored in eFuse.

Chapter 3
Power Management

This chapter covers the following topics:

- Power-up Sequence and Reset
- Device Reset

3.1 Power-up Sequence and Reset

3.1.1 Power-Up and Reset Timing

"Figure 3-1." describes the proper timing for power-up and reset of the MLSoC.

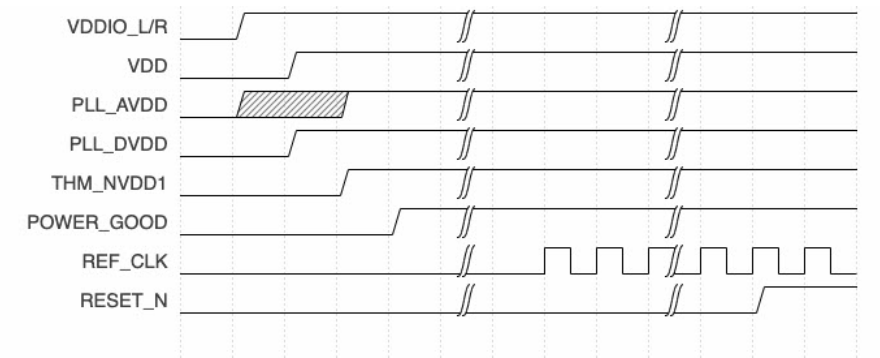


Figure 3-1. MLSoC Power-Up and Reset Timing Diagram

The timing diagram above describes the following sequencing:

- The VDDIO_x supply comes up first.
- The VDD and PLL_DVDD come up next.
  - Once stable, the POC circuit in the pad segments detects that both VDDIO and VDD are valid and enable the pads.
  - The internal POR triggers when VDD reaches a threshold and then deasserts an internal reset.
- Then THM_NVDD1 (supply to the Thermal Monitor is brought up).
- The PLL_AVDD supply for the PLLs can come up with the IO or the Thermal Monitor.
- The PMIC Power Good signal is asserted once all the supplies are valid.
- The REF clock can come up at any time after the VDDIO_L/R.
- The RESET_N must be held for the startup time of the External Crystal Oscillator OSC providing the REF_CLK time to stabilize.
- Internal reset signals are delayed, debounce the RESET_N signal.

The rise time of the supplies should be > 200us.

The various high-speed interface PHYs do not have a power supply sequencing requirement at power up. Those interfaces are enabled by the application software.

3.1.2 Power Down

Power can be turned off in the reverse sequence it was turned on, or simultaneously.

3.1.3 Recommended Power Supply Distribution

When designing for optimal power consumption, it is recommended that the 1.8V, 1.1V, and 0.84V power rails be derived from the same PMIC (Power Management Integrated Circuits) using individual filter circuits. Each power rail/supply can be distributed as shown below.

- PMIC with power supply of 1.8V can be distributed to (each with its own filter circuit):
  - MLSoC VDD
  - VDDIO
  - DDR VDD1
  - ETH_VPH
  - PCIe_VPH
  - THM_NVDD1
  - PLL_AVDD
  - LPDDR4 VDD1
  - Peripheral devices including SPI FLASH and eMMC
- PMIC with power supply of 1.1V can be distributed to (each with its own filter circuit):
  - MLSoC VDDQ
  - VDD2
  - LPDDR4 VDDQ
- PMIC with power supply of 0.84V can be distributed to (each with its own filter circuit):
  - MLSoC VDD
  - DDR VDD
  - PCIe_VP
  - PLL_DVDD
  - ETH_VP
  - LPDDR4 VDD

NOTE For additional details on power management, see the MLSoC PCIe HHHL or DualM.2 Board Hardware Reference Manuals and Reference Schematics.

3.2 Device Reset

The MLSoC has an external reset signal, RESET_N, to place the device in reset when asserted low. The user is required to deassert RESET_N only after power supplies are stable and within legal limits and REF_CLK is present and stable.

When RESET_N is asserted (low), the MLSoC enters reset asynchronously. When RESET_N is deasserted (high), the MLSoC is brought out of reset synchronously with REF_CLK.

Chapter 4
AC and DC Timing Characteristics

This chapter describes the AC and DC timing characteristics of the MLSoC SM1 device.

4.1 SPI Interface Timing

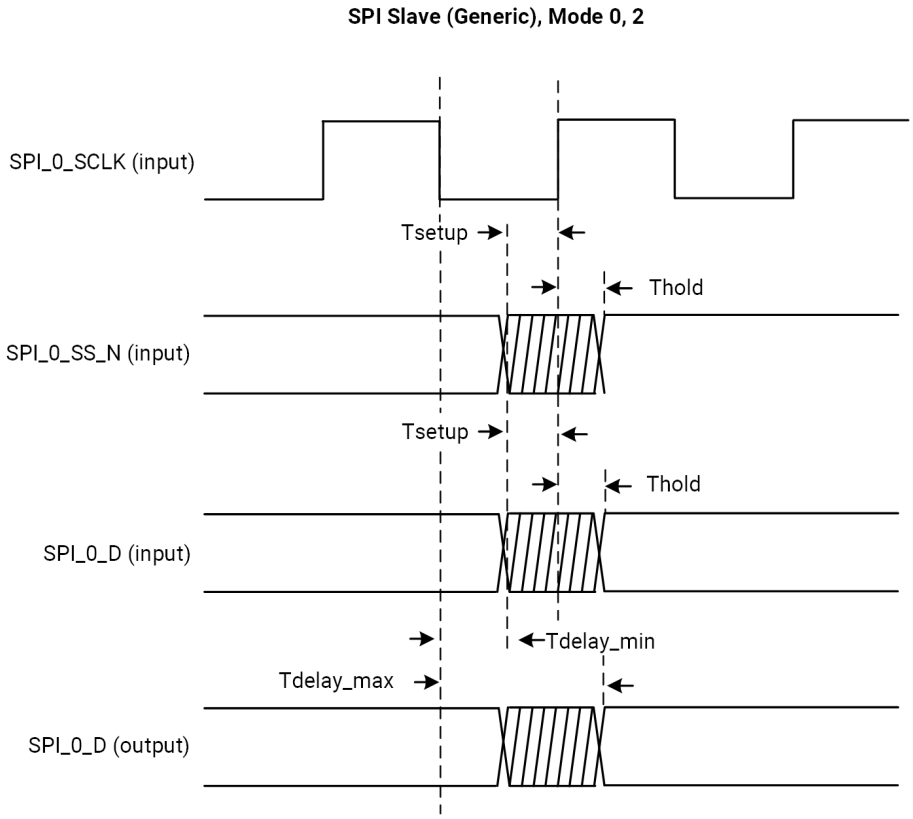


Figure 4-1. SPI Slave (Generic) Modes 0 and 2

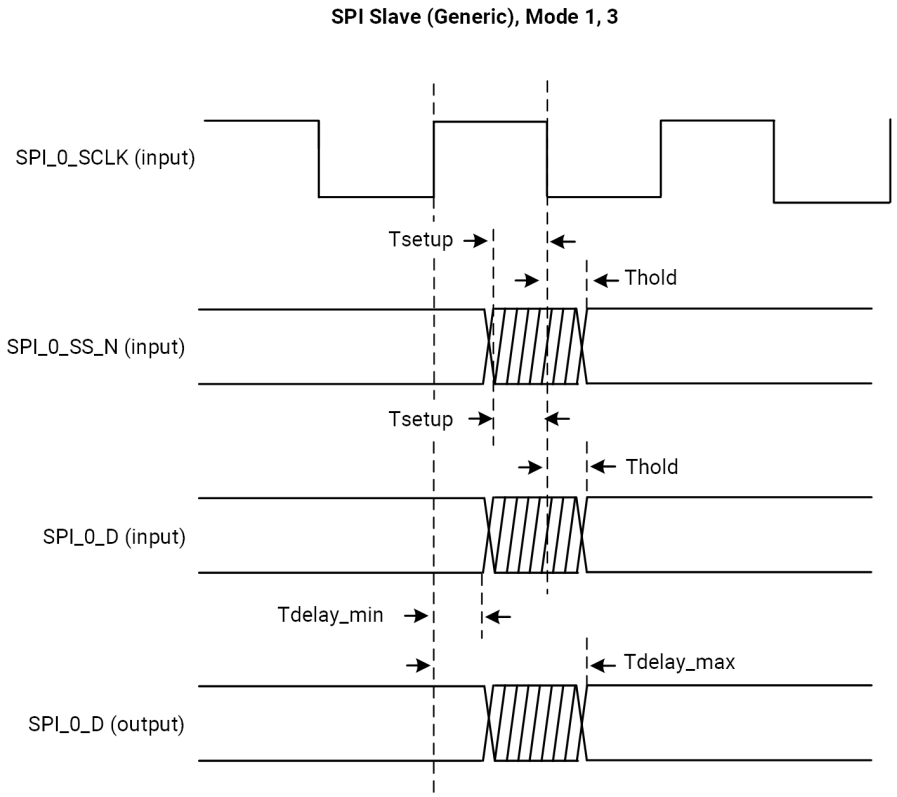


Figure 4-2. SPI Slave Modes (Generic) 1 and 3

The interface timing diagram shown above is for the SPI_0 interface. The SPI_1 is similar.

Table 4-1. Generic Slave I/F Timing

Signal	Direction	Max Freq. (MHz)	Setup Time (ns)	Hold Time (ns)	Clock Ref. (Input)	Output Delay (ns)		Clock Ref. (Output)
						Max	Min	
SPI_0_SCLK SPI_1_SCLK	Clock	25	-	-	-	-	-	-
SPI_0_SS_N[3:0] SPI_1_SS_N[3:0]	Input		10	0	SPI_0_SCLK SPI_1_SCLK	-		-
SPI_0_D[7:0] SPI_1_D[7:0]	Bidir.		3	3	SPI_0_SCLK SPI_1_SCLK	6	2	SPI_0_SCLK SPI_1_SCLK

See **"Figure 4-3."** for SPI Master (Generic) Modes 0, 2.

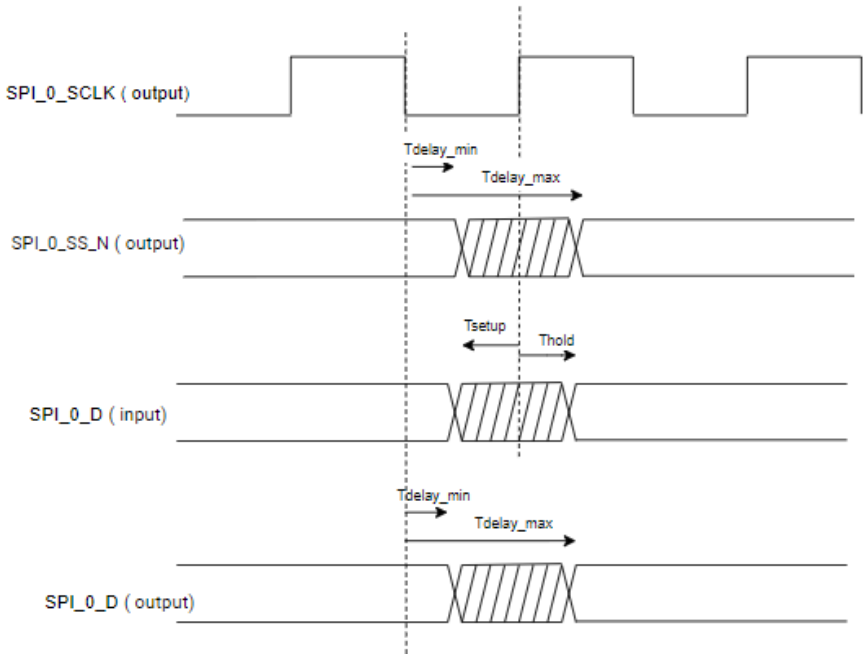


Figure 4-3. SPI Master (Generic) Modes 0, 2

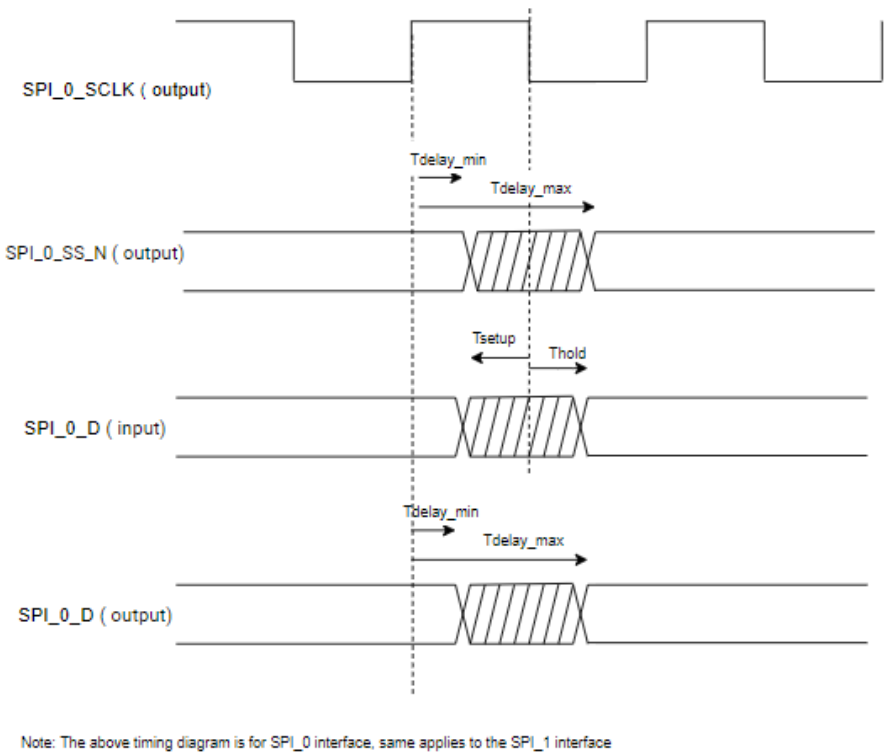


Figure 4-4. SPI Master (Generic) Modes 1, 3

Table 4-2. Generic Master I/F Timing

Signal	Direction	Max Freq. (MHz)	Setup Time (ns)	Hold Time (ns)	Clock Ref. (Input)	Output Delay (ns)		Clock Ref. (Output)
						Max	Min	
SPI_0_SCLK SPI_1_SCLK	Clock	25	-	-	-	-	-	-
SPI_0_SS_N[3:0] SPI_1_SS_N[3:0]	Output		-	-	-	3	0	SPI_0_SCLK SPI_1_SCLK
SPI_0_D[7:0] SPI_1_D[7:0]	Bidir.		10	0	SPI_0_SCLK SPI_1_SCLK	3	0	SPI_0_SCLK SPI_1_SCLK

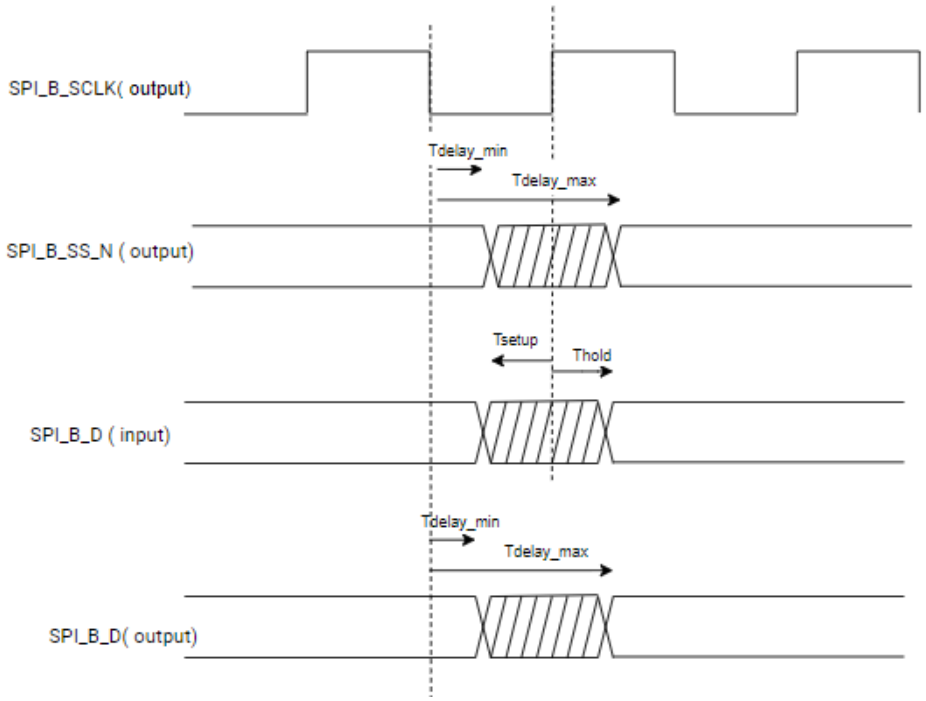


Figure 4-5. Boot Master I/F Timing (Mode 0 Only)

Table 4-3. Boot Master I/F Timing

Signal	Direction	Max Freq. (MHz)	Setup Time (ns)	Hold Time (ns)	Clock Ref. (Input)	Output Delay (ns)		Clock Ref. (Output)
						Max	Min	
SPI_B_SCLK	Clock	50	-	-	-	-	-	-
SPI_B_SS_N	Output		-	-	-	3	0	SPI_B_SCLK
SPI_B[3:0]	Bidir.		4	0	SPI_B_SCLK	3	0	SPI_B_SCLK

4.2 SDIO Interface Timing

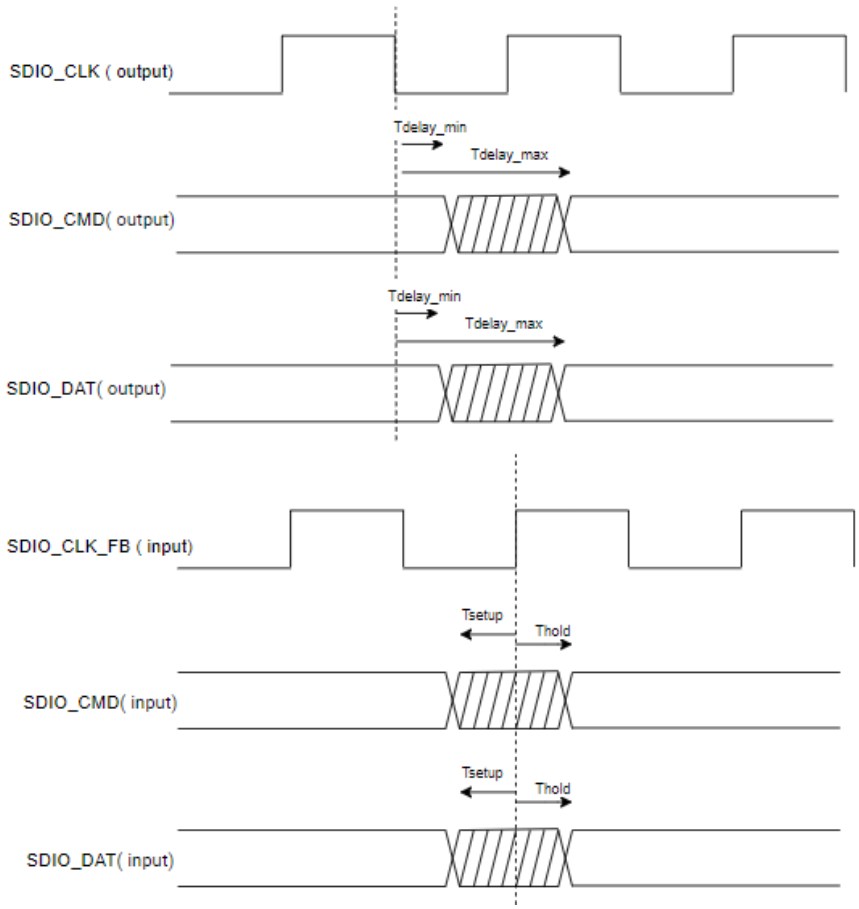


Figure 4-6. SDIO Interface

Table 4-4. SDIO Interface Timing

Signal	Direction	Max Freq. (MHz)	Setup Time (ns)	Hold Time (ns)	Clock Ref. (Input)	Output Delay (ns)		Clock Ref. (Output)
						Max	Min	
SDIO_CLK	Clock	100	-	-	-	-	-	-
SDIO_CLK_FB	Clock	100	-	-	-	-	-	-
SDIO_CMD	Bidir.		8.5	0	SDIO_CLK_FB	2	0	SDIO_CLK
SDIO_DAT	Bidir.		3.5	0	SDIO_CLK_FB	2	0	SDIO_CLK
SDIO_CRD_DET_N	Input				Async			
SDIO_CRD_WR_PROT	Input				Async			
SDIO_ENA	Output				Async			

4.3 eMMC Interface Timing

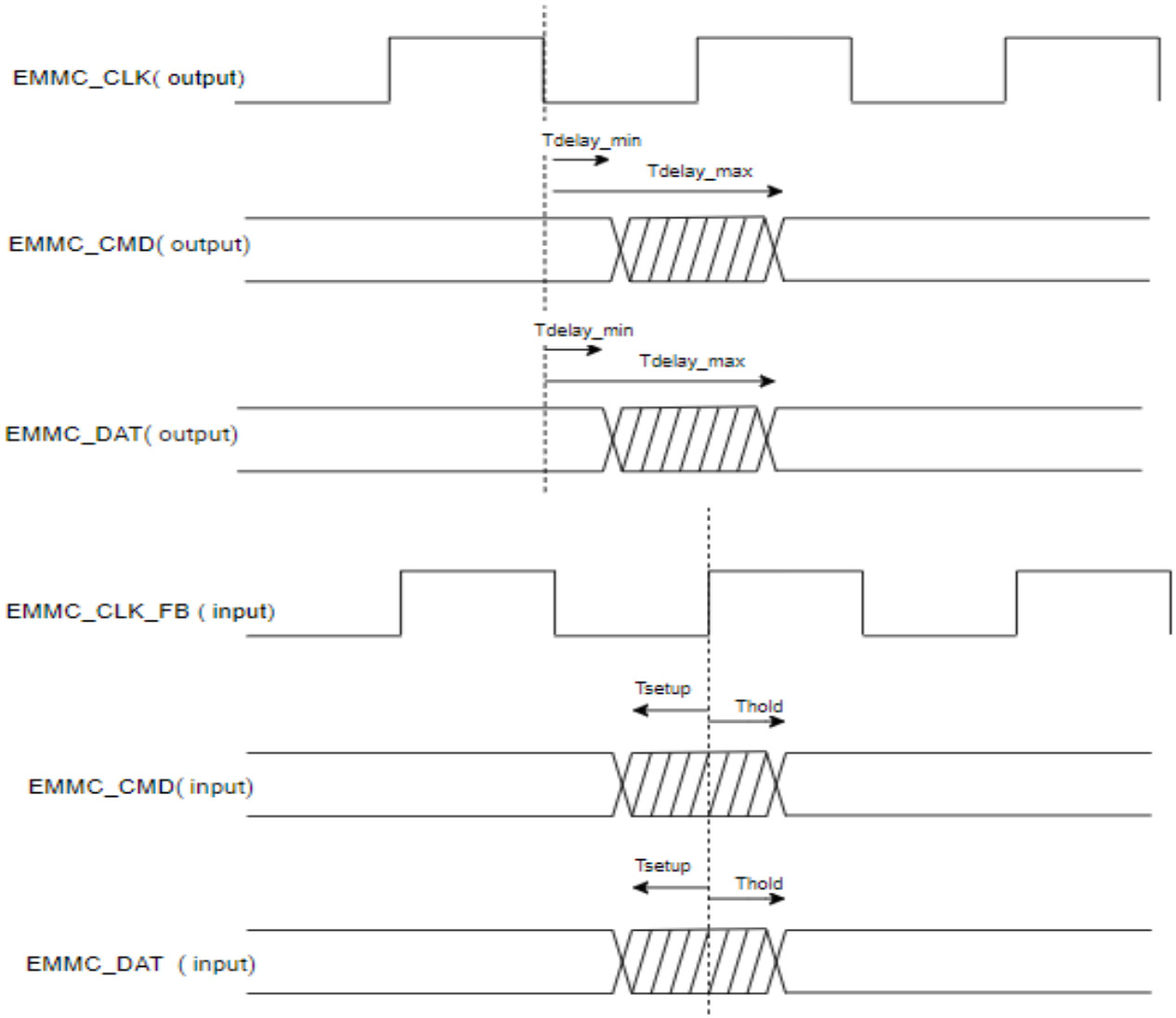


Figure 4-7. eMMC Interface

Table 4-5. eMMC Interface Timing

Signal	Direction	Max Freq. (MHz)	Setup Time (ns)	Hold Time (ns)	Clock Ref. (Input)	Output Delay (ns)		Clock Ref. (Output)
						Max	Min	
EMMC_CLK	Clock	50	-	-	-	-	-	-
EMMC_CLK_FB	Clock	50	-	-	-	-	-	-
EMMC_CMD	Bidir.		5	0.25	EMMC_CLK_FB	2	0	EMMC_CLK
EMMC_DAT	Bidir.		6	0	EMMC_CLK_FB	2	0	EMMC_CLK
EMMC_CRD_DET_N	Input				Async			
EMMC_CRD_WR_PROT	Input				Async			
EMMC_DAT_STB	Input				Unused			
EMMC_RST_N	Output				Async			

4.4 JTAG Interface Timing

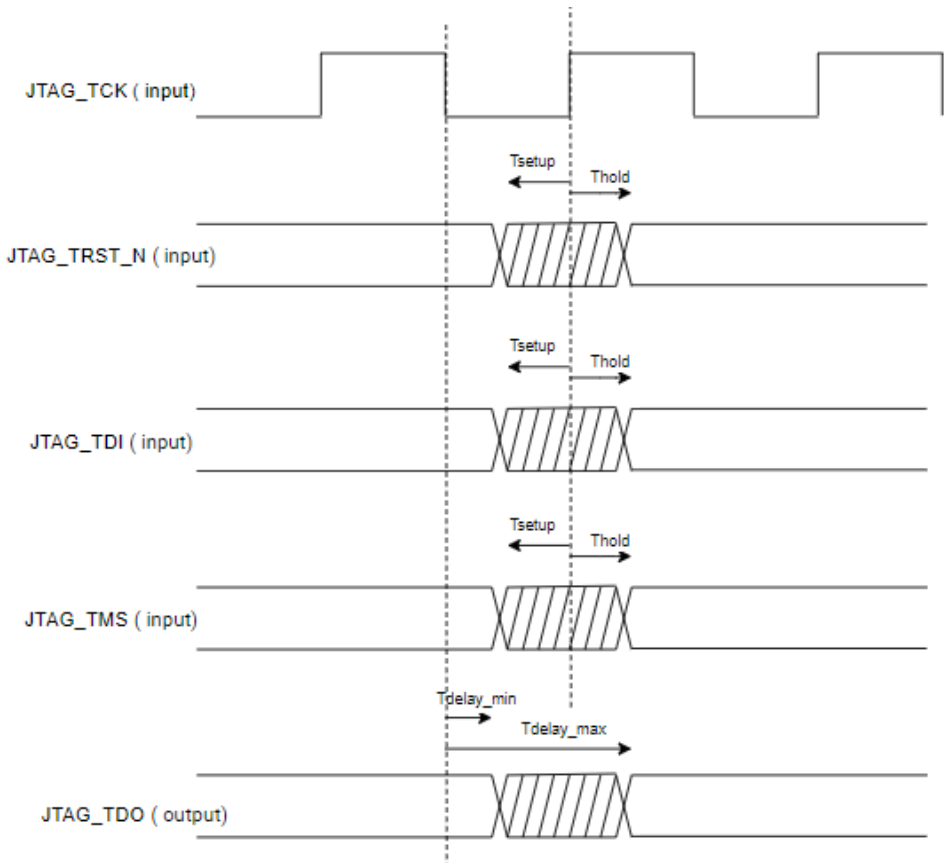


Figure 4-8. JTAG Interface

Table 4-6. JTAG Interface Timing

Signal	Direction	Max Freq. (MHz)	Setup Time (ns)	Hold Time (ns)	Clock Ref. (Input)	Output Delay (ns)		Clock Ref. (Output)
						Max	Min	
JTAG_CLK	Clock	10	-	-	-	-	-	-
JTAG_TRST_N	Input		8.5	0	JTAG_TCK	-	-	-
JTAG_TDI	Input		8.5	0	JTAG_TCK	-	-	-
JTAG_TMS	Input		8.5	0	JTAG_TCK	-	-	-
JTAG_TDO	Output		-	-	-	29	0	JTAG_TCK

4.5 Misc Signal Timing

Table 4-7. Misc. Signal Timing

Signal	Direction	Frequency (MHz)
BOOT_MODE	Input	Async
POWER_GOOD	Input	Async
RESET_N	Input	Async
SYS_STATUS	Output	Async
REF_CLK	Clock Input	33.33
RTC_CLK	Clock Input	0.032768

4.5.1 Jitter Specification Requirement

The jitter specification requirements for the MLSoC SM1 are as follows:

- 1.6 psrms (Integrated Rj from 12 KHz to 20 MHz)
- 1.2 psrms (Integrated Rj from 2 MHz to 20 MHz)
- 2.8 ps,pp (Dj, 0.75-10 MHz offset)
- 5.6 ps,pp (Dj, 0.2-50 MHz offset)

Chapter 5
Pinout and Signal Descriptions

This chapter describes the pinout and signal descriptions of the MLSoC SM1, including a color pinout layout map (see "**Figure 5-1. **").

See Table 6-1, “Nominal Voltages, Power Supplies, and Tolerance Ranges,” on page 69.

5.1 Signal Descriptions

Table 5-1. Signal Descriptions

Signal Name	Type	Description	IO Type
VDD	Supply	VDD core supply. See Table 6-1 on page 69.	PWR
VSS	Ground	VSS common ground	GND
PLL_AVDD	Supply	PLL Analog Voltage Supply. See Table 6-1 on page 69.	PWR
PLL_DVDD	Supply	PLL Digital Voltage Supply. See Table 6-1 on page 69.	PWR
PLL_VSS	Ground	PLL Ground	GND
VDDIO_L	Supply	IO supply. See Table 6-1 on page 69.	PWR
VDDIO_R	Supply	IO supply. See Table 6-1 on page 69.	PWR
VQPS	Supply	EFuse Programming Voltage supply. See Table 6-1 on page 69.	PWR
RSVD	N/A	Reserved	LVCMOS18
RSVD_0	N/A	Reserved, tie to 0V/VSS	LVCMOS18
RESET_N	IN	Power On Reset (Active low)	LVCMOS18
POWER_GOOD	IN	External power supply ready indicator (active high)	LVCMOS18
REF_CLK	IN	Reference Clock	LVCMOS18
RTC_CLK	IN	Real Time Clock OSC	LVCMOS18
BOOT_MODE[3:0]	IN	Boot mode control	LVCMOS18
SYS_STATUS[3:0]	OUT	Status output	LVCMOS18
GPIO_IO[31:18]	IO	General Purpose IO [31:18]	LVCMOS18
GPIO_IO[16:0]	IO	General Purpose IO [16:0]	LVCMOS18
SPI_B_D[3:0]	IO	Boot SPI data	LVCMOS18
SPI_B_SCLK	OUT	Boot SPI clock	LVCMOS18
SPI_B_SS_N	OUT	Boot SPI chip select	LVCMOS18

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
UART_B_RX	IN	Boot CPU UART Receiver	LVCMOS18
UART_B_TX	OUT	Boot CPU UART Transmitter	LVCMOS18
I2C_0_SCK	IO	I2C clock, interface #0	LVCMOS18
I2C_0_SDA	IO	I2C data, interface #0	LVCMOS18
I2C_1_SCK	IO	I2C clock, interface #1	LVCMOS18
I2C_1_SDA	IO	I2C data, interface #1	LVCMOS18
SPI_0_SS_N[3:0]	IO	SPI Chip select, interface #0	LVCMOS18
SPI_0_SCLK	IO	SPI clock, interface #0	LVCMOS18
SPI_0_D[7:0]	IO	SPI data, interface #0	LVCMOS18
SPI_1_SS_N[3:0]	IO	SPI Chip select, interface #1	LVCMOS18
SPI_1_SCLK	IO	SPI clock, interface #1	LVCMOS18
SPI_1_D[7:0]	IO	SPI data, interface #1	LVCMOS18
UART_0_RX	IN	UART #0 Receiver	LVCMOS18
UART_0_TX	OUT	UART #0 Transmitter	LVCMOS18
UART_1_RX	IN	UART #1 Receiver	LVCMOS18
UART_1_TX	OUT	UART #1 Transmitter	LVCMOS18
UART_2_TX	IN	UART #2 Receiver	LVCMOS18
UART_2_RX	OUT	UART #2 Transmitter	LVCMOS18
UART_3_RX	IN	UART #3 Receiver	LVCMOS18
UART_3_TX	OUT	UART #3 Transmitter	LVCMOS18
EMMC_CLK	IO	eMMC clock	LVCMOS18
EMMC_CMD	IO	eMMC Command	LVCMOS18
EMMC_DAT[7:0]	IO	eMMC Data	LVCMOS18
EMMC_CLK_FB	IN	eMMC Feedback clock	LVCMOS18
EMMC_CRD_DET_N	IN	eMMC Card Detect	LVCMOS18
EMMC_RST_N	IO	eMMC Reset	LVCMOS18
EMMC_CRD_WR_PROT	IN	eMMC Write Protect	LVCMOS18
EMMC_DAT_STB	IN	eMMC Data Strobe	LVCMOS18
SDIO_CLK	OUT	SDIO clock	LVCMOS18
SDIO_CMD	IO	SDIO command	LVCMOS18
SDIO_DAT[3:0]	IO	SDIO data	LVCMOS18
SDIO_CLK_FB	IN	SDIO feedback clock	LVCMOS18
SDIO_CRD_DET_N	IN	SDIO card detect	LVCMOS18

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
SDIO_CRD_WR_PROT	IN	SDIO Write enable	LVCMOS18
SDIO_ENA	IO	SDIO Enable	LVCMOS18
PCIE1_VP	Supply	PCIE Low Voltage Supply. See Table 6-1 on page 69.	PWR
PCIE1_VPH	Supply	PCIE High Voltage Supply. See Table 6-1 on page 69.	PWR
PCIE0_VP	Supply	PCIE Low Voltage Supply. See Table 6-1 on page 69.	PWR
PCIE0_VPH	Supply	PCIE High Voltage Supply. See Table 6-1 on page 69.	PWR
PCIE_CLK_P[1:0]/PCIE_-CLK_N[1:0]	IN	PCIe differential clock input	LVDS
PCIE_RES[1:0]	IN	PCIe reference resistor to GND. External resistor value: Precision 200 ohms (+/1%).	Analog
PCIE_TX_P[7:0]/PCIE_TX_N[7:0]	IO	8-lane PCIe differential transmitters	LVDS
PCIE_RX_P[7:0]/PCIE_RX_N[7:0]	IO	8-lane PCIe differential receivers	LVDS
ETH_VPH	Supply	Ethernet High Voltage Supply. See Table 6-1 on page 69.	PWR
ETH_VP	Supply	PCIE Low Voltage Supply. See Table 6-1 on page 69.	PWR
ETH_CLK_P/ETH_CLK_M	IN	Ethernet differential reference clock input.	LVDS
ETH_RES	IO	Ethernet reference resistor to GND. External resistor value: Precision 200 ohms (+/1%).	Analog
ETH_0_TX_P/ETH_0_TX_M	IO	Ethernet Differential Transmitter link #0	LVDS
ETH_0_RX_P/ETH_0_RX_M	IO	Ethernet Differential Receiver link #0	LVDS
ETH_1_TX_P/ETH_1_TX_M	IO	Ethernet Differential Transmitter link #1	LVDS
ETH_1_RX_P/ETH_1_RX_M	IO	Ethernet Differential Receiver link #1	LVDS
ETH_2_TX_P/ETH_2_TX_M	IO	Ethernet Differential Transmitter link #2	LVDS
ETH_2_RX_P/ETH_2_RX_M	IO	Ethernet Differential Receiver link #2	LVDS
ETH_3_TX_P/ETH_3_TX_M	IO	Ethernet Differential Transmitter link #3	LVDS
ETH_3_RX_P/ETH_3_RX_M	IO	Ethernet Differential Receiver link #3	LVDS
JTAG_TRST_N	IN	Debug JTAG interface Test Reset	LVCMOS18
JTAG_TCK	IN	Debug JTAG interface Test Clock	LVCMOS18
JTAG_TMS	IN	Debug JTAG interface Test Mode Select	LVCMOS18
JTAG_TDI	IN	Debug JTAG interface Test Data In	LVCMOS18

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
JTAG_TDO	OUT	Debug JTAG interface Test Data Out	LVCMOS18
THM_NVDD1	Supply	Thermal Monitor power supply. See Table 6-1 on page 69.	PWR
THM_VINS	IO	Thermal monitor external sense input	Analog
THM_VREFN	IO	Thermal monitor negative reference voltage	Analog
THM_VREFP	IO	Thermal monitor positive reference voltage	Analog
DDR_0_CA_A[5:0]	IO	LPDDR4 Address, Channel A, Interface 0	JEDEC Compliant
DDR_0_CKE_A[1:0]	IO	LPDDR4 clock enable, Channel A, Interface 0	JEDEC Compliant
DDR_0_CK_C_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 0	JEDEC Compliant
DDR_0_CK_T_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 0	JEDEC Compliant
DDR_0_CS_A[1:0]	IO	LPDDR4 chip select, Channel A, Interface 0	JEDEC Compliant
DDR_0_DMI_A[1:0]	IO	LPDDR4 Data mask/inversion, Channel A, Interface 0	JEDEC Compliant
DDR_0_DQS_C_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 0	JEDEC Compliant
DDR_0_DQS_T_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 0	JEDEC Compliant
DDR_0_DQ_A[15:0]	IO	LPDDR4 Data, Channel A, Interface 0	JEDEC Compliant
DDR_0_CA_B[5:0]	IO	LPDDR4 Address, Channel B, Interface 0	JEDEC Compliant
DDR_0_CKE_B[1:0]	IO	LPDDR4 clock enable, Channel B, Interface 0	JEDEC Compliant
DDR_0_CK_C_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 0	JEDEC Compliant
DDR_0_CK_T_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 0	JEDEC Compliant
DDR_0_CS_B[1:0]	IO	LPDDR4 chip select, Channel B, Interface 0	JEDEC Compliant
DDR_0_DMI_B[1:0]	IO	LPDDR4 Data mask/inversion, Channel B, Interface 0	JEDEC Compliant
DDR_0_DQS_C_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 0	JEDEC Compliant
DDR_0_DQS_T_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 0	JEDEC Compliant
DDR_0_DQ_B[15:0]	IO	LPDDR4 Data, Channel B, Interface 0	JEDEC Compliant
DDR_0_RESET_N	OUT	LPDDR4 reset, Interface 0	VDDQ

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
DDR_0_ZN	OUT	Calibration Resistor Pad, Interface 0	Analog
DDR_0_ZN_SENSE	IN	Calibration Resistor Sense Pad, Interface 0	Analog
DDR_0_ALERT_N	IO	DPHY ALERT signal, Interface 0	VDDQ
DDR_0_VREF	IO	Vref Input varies, Interface 0	Analog
DDR_0_VAA	Supply	DRAM LPDDR4 PLL Supply Interface 0. See Table 6-1 on page 69.	PWR
DDR_0_VDD	Supply	DRAM LPDDR4 Logic Supply Interface 0. See Table 6-1 on page 69.	PWR
DDR_0_VDDQ	Supply	DRAM LPDDR4 IO Supply Interface 0. See Table 6-1 on page 69.	PWR
DDR_1_CA_A[5:0]	IO	LPDDR4 Address, Channel A, Interface 1	JEDEC Compliant
DDR_1_CKE_A[1:0]	IO	LPDDR4 clock enable, Channel A, Interface 1	JEDEC Compliant
DDR_1_CK_C_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 1	JEDEC Compliant
DDR_1_CK_T_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 1	JEDEC Compliant
DDR_1_CS_A[1:0]	IO	LPDDR4 chip select, Channel A, Interface 1	JEDEC Compliant
DDR_1_DMI_A[1:0]	IO	LPDDR4 Data mask/inversion, Channel A, Interface 1	JEDEC Compliant
DDR_1_DQS_C_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 1	JEDEC Compliant
DDR_1_DQS_T_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 1	JEDEC Compliant
DDR_1_DQ_A[15:0]	IO	LPDDR4 Data, Channel A, Interface 1	JEDEC Compliant
DDR_1_CA_B[5:0]	IO	LPDDR4 Address, Channel B, Interface 1	JEDEC Compliant
DDR_1_CKE_B[1:0]	IO	LPDDR4 clock enable, Channel B, Interface 1	JEDEC Compliant
DDR_1_CK_C_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 1	JEDEC Compliant
DDR_1_CK_T_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 1	JEDEC Compliant
DDR_1_CS_B[1:0]	IO	LPDDR4 chip select, Channel B, Interface 1	JEDEC Compliant
DDR_1_DMI_B[1:0]	IO	LPDDR4 Data mask/inversion, Channel B, Interface 1	JEDEC Compliant
DDR_1_DQS_C_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 1	JEDEC Compliant
DDR_1_DQS_T_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 1	JEDEC Compliant

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
DDR_1_DQ_B[15:0]	IO	LPDDR4 Data, Channel B, Interface 1	JEDEC Compliant
DDR_1_RESET_N	OUT	LPDDR4 reset, Interface 1	VDDQ
DDR_1_ZN	OUT	Calibration Resistor Pad Interface 1	Analog
DDR_1_ZN_SENSE	IN	Calibration Resistor Sense Pad, Interface 1	Analog
DDR_1_ALERT_N	IO	DPHY ALERT signal, Interface 1	VDDQ
DDR_1_VREF	IO	Vref Input varies, Interface 1	Analog
DDR_1_VAA	Supply	DRAM LPDDR4 PLL Supply Interface 1. See Table 6-1 on page 69.	PWR
DDR_1_VDD	Supply	DRAM LPDDR4 Logic Supply Interface 1. See Table 6-1 on page 69.	PWR
DDR_1_VDDQ	Supply	DRAM LPDDR4 IO Supply Interface 1. See Table 6-1 on page 69.	PWR
DDR_2_CA_A[5:0]	IO	LPDDR4 Address, Channel A, Interface 2	JEDEC Compliant
DDR_2_CKE_A[1:0]	IO	LPDDR4 clock enable, Channel A, Interface 2	JEDEC Compliant
DDR_2_CK_C_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 2	JEDEC Compliant
DDR_2_CK_T_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 2	JEDEC Compliant
DDR_2_CS_A[1:0]	IO	LPDDR4 chip select, Channel A, Interface 2	JEDEC Compliant
DDR_2_DMI_A[1:0]	IO	LPDDR4 Data mask/inversion, Channel A, Interface 2	JEDEC Compliant
DDR_2_DQS_C_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 2	JEDEC Compliant
DDR_2_DQS_T_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 2	JEDEC Compliant
DDR_2_DQ_A[15:0]	IO	LPDDR4 Data, Channel A, Interface 2	JEDEC Compliant
DDR_2_CA_B[5:0]	IO	LPDDR4 Address, Channel B, Interface 2	
DDR_2_CKE_B[1:0]	IO	LPDDR4 clock enable, Channel B, Interface 2	
DDR_2_CK_C_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 2	JEDEC Compliant
DDR_2_CK_T_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 2	JEDEC Compliant
DDR_2_CS_B[1:0]	IO	LPDDR4 chip select, Channel B, Interface 2	JEDEC Compliant
DDR_2_DMI_B[1:0]	IO	LPDDR4 Data mask/inversion, Channel B, Interface 2	JEDEC Compliant

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
DDR_2_DQS_C_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 2	JEDEC Compliant
DDR_2_DQS_T_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 2	JEDEC Compliant
DDR_2_DQ_B[15:0]	IO	LPDDR4 Data, Channel B, Interface 2	JEDEC Compliant
DDR_2_RESET_N	OUT	LPDDR4 reset, Interface 2	VDDQ
DDR_2_ZN	OUT	Calibration Resistor Pad Interface 2	Analog
DDR_2_ZN_SENSE	IN	Calibration Resistor. Sense Pad, Interface 2	Analog
DDR_2_ALERT_N	IO	DPHY ALERT signal, Interface 2	VDDQ
DDR_2_VREF	IO	Vref Input varies, Interface 2	Analog
DDR_2_VAA	Supply	DRAM LPDDR4 PLL Supply Interface 2. See Table 6-1 on page 69.	PWR
DDR_2_VDD	Supply	DRAM LPDDR4 Logic Supply interface 2. See Table 6-1 on page 69.	PWR
DDR_2_VDDQ	Supply	DRAM LPDDR4 IO Supply Interface 2. See Table 6-1 on page 69.	PWR
DDR_3_CA_A[5:0]	IO	LPDDR4 Address, Channel A, Interface 3	JEDEC Compliant
DDR_3_CKE_A[1:0]	IO	LPDDR4 clock enable, Channel A, Interface 3	JEDEC Compliant
DDR_3_CK_C_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 3	JEDEC Compliant
DDR_3_CK_T_A	IO	LPDDR4 Address/Command clock, Channel A, Interface 3	JEDEC Compliant
DDR_3_CS_A[1:0]	IO	LPDDR4 chip select, Channel A, Interface 3	JEDEC Compliant
DDR_3_DMI_A[1:0]	IO	LPDDR4 Data mask/inversion, Channel A, Interface 3	JEDEC Compliant
DDR_3_DQS_C_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 3	JEDEC Compliant
DDR_3_DQS_T_A[1:0]	IO	LPDDR4 Data strobe, Channel A, Interface 3	JEDEC Compliant
DDR_3_DQ_A[15:0]	IO	LPDDR4 Data, Channel A, Interface 3	JEDEC Compliant
DDR_3_CA_B[5:0]	IO	LPDDR4 Address, Channel B, Interface 3	JEDEC Compliant
DDR_3_CKE_B[1:0]	IO	LPDDR4 clock enable, Channel B, Interface 3	JEDEC Compliant
DDR_3_CK_C_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 3	JEDEC Compliant
DDR_3_CK_T_B	IO	LPDDR4 Address/Command clock, Channel B, Interface 3	JEDEC Compliant

Table 5-1. Signal Descriptions (continued)

Signal Name	Type	Description	IO Type
DDR_3_CS_B[1:0]	IO	LPDDR4 chip select, Channel B, Interface 3	JEDEC Compliant
DDR_3_DMI_B[1:0]	IO	LPDDR4 Data mask/inversion, Channel B, Interface 3	JEDEC Compliant
DDR_3_DQS_C_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 3	JEDEC Compliant
DDR_3_DQS_T_B[1:0]	IO	LPDDR4 Data strobe, Channel B, Interface 3	JEDEC Compliant
DDR_3_DQ_B[15:0]	IO	LPDDR4 Data, Channel B, Interface 3	JEDEC Compliant
DDR_3_RESET_N	OUT	LPDDR4 reset, Interface 3	VDDQ
DDR_3_ZN	OUT	Calibration Resistor Pad Interface 3	Analog
DDR_3_ZN_SENSE	IN	Calibration Resistor Sense Pad, Interface 3	Analog
DDR_3_ALERT_N	IO	DPHY ALERT signal, Interface 3	VDDQ
DDR_3_VREF	IO	Vref Input varies, Interface 3	Analog
DDR_3_VAA	Supply	DRAM LPDDR4 PLL Supply Interface 3. See Table 6-1 on page 69.	PWR
DDR_3_VDD	Supply	DRAM LPDDR4 Logic Supply Interface 3. See Table 6-1 on page 69.	PWR
DDR_3_VDDQ	Supply	DRAM LPDDR4 IO Supply Interface 3. See Table 6-1 on page 69.	PWR

Table 5-2. MLSoC SM1 Pin and Signal Names

Pin Name	Signal Name	Pin Name	Signal Name
A1	VSS	A30	DDR_3_CK_C_A
A2	VSS	A31	DDR_3_DQS_C_A[1]
A3	REF_CLK	A32	DDR_3_DQS_T_A[1]
A4	RESET_N	A33	DDR_3_DQ_A[12]
A5	VSS	A34	DDR_3_DQS_C_A[0]
A6	DDR_1_DMI_A[0]	A35	DDR_3_DQS_T_A[0]
A7	DDR_1_DQ_A[4]	A36	DDR_3_DQ_A[5]
A8	DDR_2_DQS_T_B[0]	A37	VSS
A9	DDR_2_DQS_C_B[0]	B1	DDR_1_DQS_T_A[0]
A10	DDR_2_DQS_T_B[1]	B2	VSS
A11	DDR_2_DQS_C_B[1]	B3	DDR_1_DQ_A[14]
A12	DDR_2_CK_C_B	B4	DDR_1_DQ_A[15]
A13	DDR_2_CK_T_B	B5	DDR_1_DQ_A[0]
A14	DDR_2_CS_B[1]	B6	VSS
A15	DDR_2_CK_T_A	B7	DDR_1_DQ_A[5]
A16	DDR_2_CK_C_A	B8	VSS
A17	DDR_2_DQS_C_A[1]	B9	DDR_2_DQ_B[3]
A18	DDR_2_DQS_T_A[1]	B10	VSS
A19	DDR_2_DQS_C_A[0]	B11	DDR_2_DQ_B[9]
A20	DDR_2_DQS_T_A[0]	B12	VSS
A21	VSS	B13	DDR_2_CA_B[5]
A22	DDR_3_DQS_T_B[0]	B14	VSS
A23	DDR_3_DQS_C_B[0]	B15	DDR_2_CS_A[0]
A24	DDR_3_DQS_T_B[1]	B16	VSS
A25	DDR_3_DQS_C_B[1]	B17	DDR_2_DQ_A[9]
A26	DDR_3_CK_C_B	B18	VSS
A27	DDR_3_CK_T_B	B19	DDR_2_DQ_A[15]
A28	DDR_3_CKE_B[0]	B20	VSS
A29	DDR_3_CK_T_A	B21	DDR_2_DQ_A[5]
B22	VSS	C15	DDR_2_CS_A[1]
B23	DDR_3_DQ_B[7]	C16	DDR_2_CA_A[3]

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
B24	VSS	C17	DDR_2_CKE_A[0]
B25	DDR_3_DQ_B[12]	C18	DDR_2_DQ_A[8]
B26	VSS	C19	DDR_2_DQ_A[14]
B27	DDR_3_CA_B[1]	C20	DDR_2_DQ_A[1]
B28	VSS	C21	DDR_2_DQ_A[3]
B29	DDR_3_CS_A[0]	C22	DDR_3_DQ_B[5]
B30	VSS	C23	DDR_3_DMI_B[0]
B31	DDR_3_CA_A[3]	C24	DDR_3_DQ_B[1]
B32	VSS	C25	DDR_3_DQ_B[9]
B33	DDR_3_DMI_A[1]	C26	DDR_3_DQ_B[10]
B34	VSS	C27	DDR_3_CKE_B[1]
B35	DDR_3_DQ_A[2]	C28	DDR_3_ZN
B36	DDR_3_DQ_A[3]	C29	DDR_3_RESET_N
B37	DDR_3_DMI_A[0]	C30	DDR_3_CA_A[5]
C1	DDR_1_DQS_C_A[0]	C31	DDR_3_CA_A[4]
C2	DDR_1_DQ_A[10]	C32	DDR_3_CA_A[0]
C3	DDR_1_DQ_A[13]	C33	DDR_3_DQ_A[11]
C4	DDR_1_DQ_A[12]	C34	DDR_3_DQ_A[14]
C5	DDR_1_DQ_A[1]	C35	DDR_3_DQ_A[0]
C6	DDR_1_DQ_A[3]	C36	DDR_3_DQ_A[6]
C7	DDR_1_DQ_A[6]	C37	DDR_3_DQ_A[7]
C8	DDR_2_DQ_B[2]	C14	DDR_2_CS_B[0]
C9	DDR_2_DQ_B[5]	C15	DDR_2_CS_A[1]
C10	DDR_2_DQ_B[1]	C16	DDR_2_CA_A[3]
C11	DDR_2_DQ_B[12]	C17	DDR_2_CKE_A[0]
C12	DDR_2_DQ_B[8]	C18	DDR_2_DQ_A[8]
C13	DDR_2_CA_B[2]	C19	DDR_2_DQ_A[14]
C14	DDR_2_CS_B[0]	C20	DDR_2_DQ_A[1]
C21	DDR_2_DQ_A[3]	D14	DDR_2_RESET_N
C22	DDR_3_DQ_B[5]	D15	DDR_2_CA_A[5]

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
C23	DDR_3_DMI_B[0]	D16	DDR_2_CA_A[2]
C24	DDR_3_DQ_B[1]	D17	DDR_2_CKE_A[1]
C25	DDR_3_DQ_B[9]	D18	DDR_2_DQ_A[10]
C26	DDR_3_DQ_B[10]	D19	DDR_2_DQ_A[13]
C27	DDR_3_CKE_B[1]	D20	DDR_2_DQ_A[2]
C28	DDR_3_ZN	D21	DDR_2_DMI_A[0]
C29	DDR_3_RESET_N	D22	DDR_3_DQ_B[6]
C30	DDR_3_CA_A[5]	D23	DDR_3_DQ_B[4]
C31	DDR_3_CA_A[4]	D24	DDR_3_DQ_B[0]
C32	DDR_3_CA_A[0]	D25	DDR_3_DMI_B[1]
C33	DDR_3_DQ_A[11]	D26	DDR_3_DQ_B[11]
C34	DDR_3_DQ_A[14]	D27	DDR_3_CA_B[0]
C35	DDR_3_DQ_A[0]	D28	DDR_3_CA_B[3]
C36	DDR_3_DQ_A[6]	D29	DDR_3_CS_B[1]
C37	DDR_3_DQ_A[7]	D30	DDR_3_ZN_SENSE
D1	DDR_1_DQS_T_A[1]	D31	DDR_3_CKE_A[0]
D2	VSS	D32	DDR_3_CKE_A[1]
D3	DDR_1_DQ_A[8]	D33	DDR_3_DQ_A[10]
D4	DDR_1_DQ_A[11]	D34	DDR_3_DQ_A[15]
D5	VSS	D35	DDR_3_DQ_A[1]
D6	DDR_1_DQ_A[2]	D36	DDR_3_DQ_A[4]
D7	DDR_1_DQ_A[7]	D37	SPI_B_D[0]
D8	DDR_2_DQ_B[4]	E1	DDR_1_DQS_C_A[1]
D9	DDR_2_DQ_B[15]	E2	DDR_1_CA_A[4]
D10	DDR_2_DMI_B[1]	E3	DDR_1_CA_A[5]
D11	DDR_2_DQ_B[10]	E4	DDR_1_CKE_A[0]
D12	DDR_2_CA_B[0]	E5	DDR_1_DQ_A[9]
D13	DDR_2_CA_B[3]	E6	DDR_1_CA_A[2]
E7	DDR_2_DQ_B[7]	E37	SPI_B_D[1]
E8	VSS	F1	DDR_1_CK_C_A

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
E9	DDR_2_DQ_B[14]	F2	VSS
E10	VSS	F3	DDR_1_CS_A[1]
E11	DDR_2_DQ_B[11]	F4	DDR_1_CA_A[3]
E12	VSS	F5	VSS
E13	DDR_2_CA_B[4]	F6	DDR_1_CKE_A[1]
E14	VSS	F7	DDR_2_DQ_B[6]
E15	DDR_2_ZN_SENSE	F8	DDR_2_DMI_B[0]
E16	VSS	F9	DDR_2_DQ_B[0]
E17	DDR_2_CA_A[0]	F10	DDR_2_DQ_B[13]
E18	VSS	F11	DDR_2_CA_B[1]
E19	DDR_2_DMI_A[1]	F12	DDR_2_CKE_B[1]
E20	VSS	F13	DDR_2_CKE_B[0]
E21	DDR_2_DQ_A[4]	F14	DDR_2_ZN
E22	VSS	F15	DDR_2_ALERT_N
E23	DDR_3_DQ_B[2]	F16	DDR_2_CA_A[4]
E24	VSS	F17	DDR_2_CA_A[1]
E25	DDR_3_DQ_B[15]	F18	DDR_2_DQ_A[11]
E26	VSS	F19	DDR_2_DQ_A[12]
E27	DDR_3_CA_B[2]	F20	DDR_2_DQ_A[0]
E28	VSS	F21	DDR_2_DQ_A[6]
E29	DDR_3_CS_B[0]	F22	DDR_2_DQ_A[7]
E30	VSS	F23	DDR_3_DQ_B[3]
E31	DDR_3_CA_A[2]	F24	DDR_3_DQ_B[13]
E32	VSS	F25	DDR_3_DQ_B[14]
E33	DDR_3_DQ_A[13]	F26	DDR_3_DQ_B[8]
E34	VSS	F27	DDR_3_CA_B[4]
E35	SPI_B_D[3]	F28	DDR_3_CA_B[5]
E36	SPI_B_D[2]	F29	DDR_3_ALERT_N
F30	DDR_3_CS_A[1]	G23	DDR_3_VDDQ
F31	DDR_3_CA_A[1]	G24	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
F32	DDR_3_DQ_A[9]	G25	DDR_3_VDDQ
F33	DDR_3_DQ_A[8]	G26	VSS
F34	SPI_B_SCLK	G27	DDR_3_VDDQ
F35	SPI_B_SS_N	G28	VSS
F36	UART_B_TX	G29	VSS
F37	VSS	G30	VSS
G1	DDR_1_CK_T_A	G31	VSS
G2	DDR_1_CS_A[0]	G32	EMMC_DAT[1]
G3	DDR_1_ZN_SENSE	G33	EMMC_CRD_DET_N
G4	DDR_1_ALERT_N	G34	EMMC_RST_N
G5	DDR_1_CA_A[0]	G35	EMMC_CRD_WR_PROT
G6	DDR_1_DMI_A[1]	G36	EMMC_DAT_STB
G7	VSS	G37	UART_B_RX
G8	VSS	H1	DDR_1_CK_T_B
G9	VDDIO_T	H2	VSS
G10	VDDIO_T	H3	DDR_1_CA_B[5]
G11	VSS	H4	DDR_1_ZN
G12	VSS	H5	VSS
G13	VSS	H6	DDR_1_CA_A[1]
G14	DDR_2_VDDQ	H7	VSS
G15	DDR_2_VDDQ	H8	DDR_1_VDDQ
G16	DDR_2_VDDQ	H9	VSS
G17	DDR_2_VDDQ	H10	PLL_VSS
G18	DDR_2_VDDQ	H11	PLL_VSS
G19	VSS	H12	PLL_VSS
G20	VSS	H13	PLL_AVDD
G21	DDR_3_VDDQ	H14	VSS
G22	VSS	H15	DDR_2_VDDQ
H16	DDR_2_VDD	J9	VSS
H17	DDR_2_VDDQ	J10	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
H18	DDR_2_VDD	J11	PLL_DVDD
H19	DDR_2_VDDQ	J12	PLL_VSS
H20	DDR_3_VDDQ	J13	PLL_AVDD
H21	DDR_3_VDD	J14	VSS
H22	DDR_3_VDDQ	J15	DDR_2_VDD
H23	DDR_3_VDD	J16	DDR_2_VDD
H24	DDR_3_VDDQ	J17	DDR_2_VDD
H25	VSS	J18	DDR_2_VDD
H26	DDR_3_VDDQ	J19	DDR_2_VDD
H27	VSS	J20	DDR_3_VDD
H28	VDD	J21	DDR_3_VDD
H29	VSS	J22	DDR_3_VDD
H30	VDD	J23	DDR_3_VDD
H31	VSS	J24	DDR_3_VDD
H32	EMMC_DAT[0]	J25	DDR_3_VDD
H33	EMMC_DAT[2]	J26	VSS
H34	EMMC_DAT[3]	J27	VDD
H35	EMMC_CLK_FB	J28	VSS
H36	EMMC_CLK	J29	VDD
H37	EMMC_CMD	J30	VSS
J1	DDR_1_CK_C_B	J31	VDD
J2	DDR_1_CA_B[2]	J32	BOOT_MODE[0]
J3	DDR_1_CA_B[3]	J33	POWER_GOOD
J4	DDR_1_RESET_N	J34	EMMC_DAT[7]
J5	DDR_1_CA_B[4]	J35	EMMC_DAT[6]
J6	DDR_1_CS_B[0]	J36	EMMC_DAT[5]
J7	DDR_1_VDDQ	J37	EMMC_DAT[4]
J8	VSS	K1	DDR_1_DQS_C_B[1]
K2	VSS	K32	RTC_CLK
K3	DDR_1_CKE_B[1]	K33	BOOT_MODE[2]

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
K4	DDR_1_CKE_B[0]	K34	BOOT_MODE[1]
K5	VSS	K35	BOOT_MODE[3]
K6	DDR_1_CS_B[1]	K36	SYS_STATUS[0]
K7	VSS	K37	SYS_STATUS[1]
K8	DDR_1_VDDQ	L1	DDR_1_DQS_T_B[1]
K9	VSS	L2	DDR_1_DQ_B[10]
K10	PLL_DVDD	L3	DDR_1_CA_B[0]
K11	PLL_DVDD	L4	DDR_1_CA_B[1]
K12	PLL_VSS	L5	DDR_1_DQ_B[9]
K13	PLL_AVDD	L6	DDR_1_DQ_B[8]
K14	VSS	L7	DDR_1_VDDQ
K15	DDR_2_VDD	L8	DDR_1_VDD
K16	VSS	L9	DDR_1_VDD
K17	DDR_2_VDD	L10	VSS
K18	VSS	L11	PLL_DVDD
K19	DDR_2_VDD	L12	PLL_VSS
K20	DDR_3_VDD	L13	PLL_AVDD
K21	VSS	L14	VSS
K22	DDR_3_VDD	L15	VSS
K23	VSS	L16	DDR_2_VAA
K24	VSS	L17	DDR_2_VREF
K25	VSS	L18	VDD
K26	VDD	L19	VSS
K27	VSS	L20	DDR_3_VAA
K28	VDD	L21	DDR_3_VREF
K29	VSS	L22	VSS
K30	VDD	L23	VSS
K31	VSS	L24	VDD
L25	VSS	M18	VSS
L26	VSS	M19	VDD

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
L27	VQPS	M20	VSS
L28	VQPS	M21	DDR_3_VAA
L29	VDD	M22	VSS
L30	VSS	M23	VSS
L31	VDD	M24	VDD
L32	RSVD_0	M25	VSS
L33	RSVD	M26	VDD
L34	RSVD	M27	VSS
L35	VSS	M28	VDD
L36	SYS_STATUS[2]	M29	VSS
L37	SYS_STATUS[3]	M30	VDD
M1	DDR_1_DQS_C_B[0]	M31	VSS
M2	VSS	M32	RSVD_0
M3	DDR_1_DQ_B[13]	M33	RSVD_0
M4	DDR_1_DQ_B[12]	M34	RSVD
M5	VSS	M35	RSVD_0
M6	DDR_1_DQ_B[11]	M36	RSVD
M7	VSS	M37	RSVD_0
M8	DDR_1_VDDQ	N1	DDR_1_DQS_T_B[0]
M9	DDR_1_VDD	N2	DDR_1_DQ_B[5]
M10	DDR_1_VDD	N3	DDR_1_DQ_B[3]
M11	VSS	N4	DDR_1_DQ_B[14]
M12	VDD	N5	DDR_1_DQ_B[15]
M13	VSS	N6	DDR_1_DMI_B[1]
M14	VDD	N7	DDR_1_VDDQ
M15	VSS	N8	DDR_1_VDD
M16	VSS	N9	DDR_1_VDD
M17	DDR_2_VAA	N10	VSS
N11	DDR_1_VREF	P4	DDR_1_DQ_B[1]
N12	VSS	P5	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
N13	VDD	P6	DDR_1_DQ_B[0]
N14	VSS	P7	VSS
N15	VDD	P8	DDR_1_VDDQ
N16	VSS	P9	DDR_1_VDD
N17	VDD	P10	DDR_1_VDD
N18	VSS	P11	DDR_1_VAA
N19	VDD	P12	DDR_1_VAA
N20	VSS	P13	VSS
N21	VDD	P14	VDD
N22	VSS	P15	VSS
N23	VDD	P16	VDD
N24	VSS	P17	VSS
N25	VDD	P18	VDD
N26	VSS	P19	VSS
N27	VDD	P20	VDD
N28	VSS	P21	VSS
N29	VDD	P22	VDD
N30	VSS	P23	VSS
N31	VDDIO_L	P24	VDD
N32	RSVD	P25	VSS
N33	RSVD	P26	VDD
N34	VSS	P27	VSS
N35	RSVD	P28	VDD
N36	RSVD	P29	VSS
N37	VSS	P30	VDDIO_L
P1	DDR_1_DQ_B[4]	P31	VSS
P2	VSS	P32	RSVD
P3	DDR_1_DQ_B[2]	P33	RSVD
P34	RSVD	R27	VDD
P35	RSVD	R28	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
P36	RSVD	R29	VDD
P37	RSVD	R30	VSS
R1	VSS	R31	VDDIO_L
R2	DDR_1_DMI_B[0]	R32	RSVD
R3	DDR_1_DQ_B[7]	R33	RSVD
R4	DDR_1_DQ_B[6]	R34	RSVD
R5	DDR_0_DMI_A[0]	R35	RSVD
R6	DDR_0_DQ_A[6]	R36	RSVD
R7	DDR_1_VDDQ	R37	RSVD
R8	DDR_1_VDD	T1	DDR_0_DQS_T_A[0]
R9	DDR_1_VDD	T2	VSS
R10	VSS	T3	DDR_0_DQ_A[7]
R11	VDD	T4	DDR_0_DQ_A[5]
R12	VSS	T5	VSS
R13	VDD	T6	DDR_0_DQ_A[4]
R14	VSS	T7	VSS
R15	VDD	T8	DDR_0_VDDQ
R16	VSS	T9	DDR_0_VDD
R17	VDD	T10	DDR_0_VDD
R18	VSS	T11	VSS
R19	VDD	T12	VDD
R20	VSS	T13	VSS
R21	VDD	T14	VDD
R22	VSS	T15	VSS
R23	VDD	T16	VDD
R24	VSS	T17	VSS
R25	VDD	T18	VDD
R26	VSS	T19	VSS
T20	VDD	U13	VDD
T21	VSS	U14	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
T22	VDD	U15	VDD
T23	VSS	U16	VSS
T24	VDD	U17	VDD
T25	VSS	U18	VSS
T26	VDD	U19	VDD
T27	VSS	U20	VSS
T28	VDD	U21	VDD
T29	VSS	U22	VSS
T30	VDDIO_L	U23	VDD
T31	VSS	U24	VSS
T32	RSVD	U25	VDD
T33	RSVD	U26	VSS
T34	RSVD	U27	VDD
T35	RSVD	U28	VSS
T36	RSVD	U29	VDD
T37	RSVD	U30	VSS
U1	DDR_0_DQS_C_A[0]	U31	VDDIO_L
U2	DDR_0_DQ_A[3]	U32	RSVD
U3	DDR_0_DQ_A[1]	U33	RSVD
U4	DDR_0_DQ_A[2]	U34	RSVD
U5	DDR_0_DQ_A[0]	U35	RSVD
U6	DDR_0_DQ_A[13]	U36	RSVD
U7	DDR_0_VDDQ	U37	RSVD
U8	DDR_0_VDD	V1	DDR_0_DQS_T_A[1]
U9	DDR_0_VDD	V2	VSS
U10	VSS	V3	DDR_0_DQ_A[10]
U11	VDD	V4	DDR_0_DMI_A[1]
U12	VSS	V5	VSS
V6	DDR_0_DQ_A[14]	V35	RSVD
V6	DDR_0_DQ_A[14]	V36	RSVD

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
V7	VSS	V37	VSS
V8	DDR_0_VDDQ	W1	DDR_0_DQS_C_A[1]
V9	DDR_0_VDD	W2	DDR_0_DQ_A[9]
V10	DDR_0_VDD	W3	DDR_0_DQ_A[8]
V11	DDR_0_VREF	W4	DDR_0_DQ_A[11]
V12	DDR_0_VAA	W5	DDR_0_DQ_A[12]
V13	VSS	W6	DDR_0_DQ_A[15]
V14	VDD	W7	DDR_0_VDDQ
V15	VSS	W8	DDR_0_VDD
V16	VDD	W9	DDR_0_VDD
V17	VSS	W10	VSS
V18	VDD	W11	DDR_0_VAA
V19	VSS	W12	VSS
V20	VDD	W13	VDD
V21	VSS	W14	VSS
V22	VDD	W15	VDD
V23	VSS	W16	VSS
V24	VDD	W17	VDD
V25	VSS	W18	VSS
V26	VDD	W19	VDD
V27	VSS	W20	VSS
V28	VDD	W21	VDD
V29	VSS	W22	VSS
V30	VDDIO_L	W23	VDD
V31	VSS	W24	VSS
V32	RSVD	W25	VDD
V33	RSVD	W26	VSS
V34	VSS	W27	VDD
W28	VSS	AA21	VDD
W29	VDD	AA22	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
Y30	VDDIO_L	AA23	VDD
Y31	VSS	AA24	VSS
Y32	RSVD	AA25	VDD
Y33	RSVD	AA26	VSS
Y34	RSVD	AA27	VDD
Y35	RSVD	AA28	VSS
Y36	RSVD	AA29	VDD
Y37	RSVD	AA30	VSS
AA1	DDR_0_CK_C_A	AA31	VDD
AA2	DDR_0_CS_A[1]	AA32	RSVD
AA3	DDR_0_CA_A[5]	AA33	RSVD
AA4	DDR_0_CA_A[3]	AA34	RSVD
AA5	DDR_0_CKE_A[0]	AA35	RSVD
AA6	DDR_0_CA_A[1]	AA36	RSVD
AA7	DDR_0_VDDQ	AA37	RSVD
AA8	VSS	AB1	DDR_0_CK_T_A
AA9	VDD	AB2	VSS
AA10	VSS	AB3	DDR_0_CS_A[0]
AA11	VDD	AB4	DDR_0_RESET_N
AA12	VSS	AB5	VSS
AA13	VDD	AB6	DDR_0_ALERT_N
AA14	VSS	AB7	VSS
AA15	VDD	AB8	DDR_0_VDDQ
AA16	VSS	AB9	VSS
AA17	VDD	AB10	VDD
AA18	VSS	AB11	VSS
AA19	VDD	AB12	VDD
AA20	VSS	AB13	VSS
AB14	VDD	AC7	DDR_0_VDDQ
AB15	VSS	AC8	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AB16	VDD	AC9	VDD
AB17	VSS	AC10	VSS
AB18	VDD	AC11	VDD
AB19	VSS	AC12	VSS
AB20	VDD	AC13	VDD
AB21	VSS	AC14	VSS
AB22	VDD	AC15	VDD
AB23	VSS	AC16	VSS
AB24	VDD	AC17	VDD
AB25	VSS	AC18	VSS
AB26	VDD	AC19	VDD
AB27	VSS	AC20	VSS
AB28	VDD	AC21	VDD
AB29	VSS	AC22	VSS
AB30	VDD	AC23	VDD
AB31	VSS	AC24	VSS
AB32	RSVD	AC25	VDD
AB33	RSVD	AC26	VSS
AB34	GPIO_IO[1]	AC27	VDD
AB35	GPIO_IO[0]	AC28	VSS
AB36	GPIO_IO[2]	AC29	VDD
AB37	GPIO_IO[3]	AC30	VSS
AC1	DDR_0_CK_C_B	AC31	VDD
AC2	DDR_0_CA_B[3]	AC32	GPIO_IO[8]
AC3	DDR_0_CA_B[5]	AC33	GPIO_IO[6]
AC4	DDR_0_CS_B[1]	AC34	VSS
AC5	DDR_0_ZN	AC35	GPIO_IO[5]
AC6	DDR_0_ZN_SENSE	AC36	GPIO_IO[4]
AC37	VSS	AD30	VDD
AD1	DDR_0_CK_T_B	AD31	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AD2	VSS	AD32	GPIO_IO[7]
AD3	DDR_0_CA_B[4]	AD33	GPIO_IO[10]
AD4	DDR_0_CKE_B[1]	AD34	GPIO_IO[9]
AD5	VSS	AD35	GPIO_IO[11]
AD6	DDR_0_CS_B[0]	AD36	GPIO_IO[12]
AD7	VSS	AD37	GPIO_IO[13]
AD8	VDDIO_R	AE1	DDR_0_CA_B[0]
AD9	VSS	AE2	DDR_0_DQ_B[9]
AD10	VDD	AE3	DDR_0_CA_B[2]
AD11	VSS	AE4	DDR_0_CKE_B[0]
AD12	VDD	AE5	DDR_0_DQ_B[8]
AD13	VSS	AE6	DDR_0_CA_B[1]
AD14	VDD	AE7	VDDIO_R
AD15	VSS	AE8	VSS
AD16	VDD	AE9	VSS
AD17	VSS	AE10	VSS
AD18	VDD	AE11	VDD
AD19	VSS	AE12	VSS
AD20	VDD	AE13	VDD
AD21	VSS	AE14	VSS
AD22	VDD	AE15	VDD
AD23	VSS	AE16	VSS
AD24	VDD	AE17	VDD
AD25	VSS	AE18	VSS
AD26	VDD	AE19	VDD
AD27	VSS	AE20	VSS
AD28	VDD	AE21	VDD
AD29	VSS	AE22	VSS
AE23	VDD	AF18	VDD
AE24	VSS	AF19	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AE25	VDD	AF20	VDD
AE26	VSS	AF21	PCIE1_VP
AE27	VDD	AF22	PCIE1_VP
AE28	VSS	AF23	PCIE1_VPH
AE29	VDD	AF24	PCIE0_VPH
AE30	VSS	AF25	PCIE0_VP
AE31	VDD	AF26	PCIE0_VP
AE32	GPIO_IO[19]	AF27	VSS
AE33	GPIO_IO[18]	AF28	VDD
AE34	RSVD	AF29	VSS
AE35	GPIO_IO[16]	AF30	VDD
AE36	GPIO_IO[14]	AF31	VSS
AE37	GPIO_IO[15]	AF32	GPIO_IO[21]
AF1	DDR_0_DQS_C_B[1]	AF33	GPIO_IO[20]
AF2	VSS	AF34	GPIO_IO[22]
AF3	DDR_0_DQ_B[11]	AF35	GPIO_IO[23]
AF4	DDR_0_DQ_B[10]	AF36	GPIO_IO[24]
AF5	VSS	AF37	GPIO_IO[25]
AF6	DDR_0_DQ_B[12]	AG1	DDR_0_DQS_T_B[1]
AF7	VSS	AG2	DDR_0_DMI_B[1]
AF8	VDDIO_R	AG3	DDR_0_DQ_B[13]
AF9	THM_NVDD1	AG4	DDR_0_DQ_B[15]
AF10	THM_VINS	AG5	DDR_0_DQ_B[0]
AF11	ETH_VPH	AG6	DDR_0_DQ_B[14]
AF12	ETH_VP	AG7	VDDIO_R
AF13	ETH_VP	AG8	VSS
AF14	VDD	AG9	THM_NVDD1
AF15	VSS	AG10	THM_VREFN
AF16	VDD	AG11	ETH_VPH
AF17	VSS	AG12	ETH_VP
AG13	ETH_VP	AH8	VDDIO_R
AG14	VSS	AH9	VSS
AG15	VDD	AH10	THM_VREFP

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AG16	VSS	AH11	ETH_VPH
AG17	VDD	AH12	ETH_VP
AG18	VSS	AH13	ETH_VP
AG19	VDD	AH14	VDD
AG20	VSS	AH15	VSS
AG21	PCIE1_VP	AH16	VDD
AG22	PCIE1_VP	AH17	VSS
AG23	PCIE1_VPH	AH18	VDD
AG24	PCIE0_VPH	AH19	VSS
AG25	PCIE0_VP	AH20	VDD
AG26	PCIE0_VP	AH21	PCIE1_VP
AG27	VDD	AH22	PCIE1_VP
AG28	VSS	AH23	PCIE1_VPH
AG29	VDD	AH24	PCIE0_VPH
AG30	VSS	AH25	PCIE0_VP
AG31	VDD	AH26	PCIE0_VP
AG32	GPIO_IO[31]	AH27	VSS
AG33	GPIO_IO[30]	AH28	VDD
AG34	GPIO_IO[29]	AH29	VSS
AG35	GPIO_IO[28]	AH30	VDD
AG36	GPIO_IO[26]	AH31	VSS
AG37	GPIO_IO[27]	AH32	VDD
AH1	DDR_0_DQS_C_B[0]	AH33	VSS
AH2	VSS	AH34	VDD
AH3	DDR_0_DQ_B[1]	AH35	VSS
AH4	DDR_0_DQ_B[3]	AH36	VDD
AH5	VSS	AH37	VSS
AH6	DDR_0_DQ_B[2]	AJ1	DDR_0_DQS_T_B[0]
AH7	VSS	AJ2	DDR_0_DQ_B[5]
AJ3	DDR_0_DQ_B[4]	AJ35	VDD
AJ4	DDR_0_DMI_B[0]	AJ36	VSS
AJ5	UART_3_RX	AJ37	VDD
AJ6	UART_3_TX	AK1	DDR_0_DQ_B[7]

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AJ7	VDDIO_R	AK2	DDR_0_DQ_B[6]
AJ8	VSS	AK3	UART_1_RX
AJ9	VSS	AK4	UART_1_TX
AJ10	VSS	AK5	UART_2_TX
AJ11	ETH_VPH	AK6	UART_2_RX
AJ12	ETH_VP	AK7	VSS
AJ13	ETH_VP	AK8	VSS
AJ14	VSS	AK9	VSS
AJ15	VDD	AK10	VSS
AJ16	VSS	AK11	VSS
AJ17	VDD	AK12	VSS
AJ18	VSS	AK13	VSS
AJ19	VDD	AK14	VSS
AJ20	VSS	AK15	VSS
AJ21	PCIE1_VP	AK16	VSS
AJ22	PCIE1_VP	AK17	VSS
AJ23	PCIE1_VPH	AK18	VSS
AJ24	PCIE0_VPH	AK19	VSS
AJ25	PCIE0_VP	AK20	VSS
AJ26	PCIE0_VP	AK21	VSS
AJ27	VDD	AK22	VSS
AJ28	VSS	AK23	VSS
AJ29	VDD	AK24	VSS
AJ30	VSS	AK25	VSS
AJ31	VDD	AK26	VSS
AJ32	VSS	AK27	VSS
AJ33	VDD	AK28	VSS
AJ34	VSS	AK29	VSS
AK30	VDD	AL25	PCIE_CLK_P[0]
AK31	VSS	AL26	PCIE_CLK_N[0]
AK32	VDD	AL27	VSS
AK33	VSS	AL28	PCIE_RES[0]
AK34	VDD	AL29	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AK35	VSS	AL30	VSS
AK36	VDD	AL31	VDD
AK37	VSS	AL32	VSS
AL1	UART_0_TX	AL33	VDD
AL2	VSS	AL34	VSS
AL3	UART_0_RX	AL35	VDD
AL4	I2C_1_SCK	AL36	VSS
AL5	I2C_1_SDA	AL37	VDD
AL6	I2C_0_SCK	AM1	SPI_0_D[6]
AL7	VSS	AM2	SPI_0_SS_N[0]
AL8	VSS	AM3	SPI_0_SS_N[1]
AL9	VSS	AM4	SPI_0_SS_N[2]
AL10	ETH_CLK_M	AM5	SPI_0_SS_N[3]
AL11	ETH_CLK_P	AM6	I2C_0_SDA
AL12	VSS	AM7	SDIO_CLK_FB
AL13	ETH_RES	AM8	VSS
AL14	VSS	AM9	VSS
AL15	VSS	AM10	VSS
AL16	VSS	AM11	VSS
AL17	VSS	AM12	VSS
AL18	VSS	AM13	VSS
AL19	PCIE_CLK_P[1]	AM14	VSS
AL20	PCIE_CLK_N[1]	AM15	VSS
AL21	VSS	AM16	VSS
AL22	PCIE_RES[1]	AM17	VSS
AL23	VSS	AM18	VSS
AL24	VSS	AM19	VSS
AM20	VSS	AN15	VSS
AM21	VSS	AN16	ETH_0_TX_P
AM22	VSS	AN17	VSS
AM23	VSS	AN18	PCIE_TX_P[7]
AM24	VSS	AN19	VSS
AM25	VSS	AN20	PCIE_TX_P[6]

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AM26	VSS	AN21	VSS
AM27	VSS	AN22	PCIE_TX_P[5]
AM28	VSS	AN23	VSS
AM29	VSS	AN24	PCIE_TX_P[4]
AM30	VSS	AN25	VSS
AM31	VSS	AN26	PCIE_TX_P[3]
AM32	VSS	AN27	VSS
AM33	VSS	AN28	PCIE_TX_P[2]
AM34	VDD	AN29	VSS
AM35	VSS	AN30	PCIE_TX_P[1]
AM36	VDD	AN31	VSS
AM37	VSS	AN32	PCIE_TX_P[0]
AN1	SPI_0_D[7]	AN33	VSS
AN2	SPI_0_D[4]	AN34	VSS
AN3	SPI_0_D[5]	AN35	VDD
AN4	SPI_0_D[3]	AN36	VSS
AN5	SPI_0_D[2]	AN37	VDD
AN6	SDIO_DAT[1]	AP1	SPI_1_SS_N[3]
AN7	SDIO_CLK	AP2	VSS
AN8	JTAG_TDI	AP3	SPI_0_D[0]
AN9	VSS	AP4	SPI_0_D[1]
AN10	ETH_3_TX_P	AP5	VSS
AN11	VSS	AP6	SDIO_DAT[0]
AN12	ETH_2_TX_P	AP7	SDIO_CMD
AN13	VSS	AP8	JTAG_TDO
AN14	ETH_1_TX_P	AP9	VSS
AP10	ETH_3_TX_M	AR5	SPI_1_SCLK
AP11	VSS	AR6	SDIO_DAT[3]
AP12	ETH_2_TX_M	AR7	SDIO_CRD_DET_N
AP13	VSS	AR8	JTAG_TRST_N
AP14	ETH_1_TX_M	AR9	VSS
AP15	VSS	AR10	VSS
AP16	ETH_0_TX_M	AR11	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AP17	VSS	AR12	VSS
AP18	PCIE_TX_N[7]	AR13	VSS
AP19	VSS	AR14	VSS
AP20	PCIE_TX_N[6]	AR15	VSS
AP21	VSS	AR16	VSS
AP22	PCIE_TX_N[5]	AR17	VSS
AP23	VSS	AR18	VSS
AP24	PCIE_TX_N[4]	AR19	VSS
AP25	VSS	AR20	VSS
AP26	PCIE_TX_N[3]	AR21	VSS
AP27	VSS	AR22	VSS
AP28	PCIE_TX_N[2]	AR23	VSS
AP29	VSS	AR24	VSS
AP30	PCIE_TX_N[1]	AR25	VSS
AP31	VSS	AR26	VSS
AP32	PCIE_TX_N[0]	AR27	VSS
AP33	VSS	AR28	VSS
AP34	VDD	AR29	VSS
AP35	VSS	AR30	VSS
AP36	VDD	AR31	VSS
AP37	VSS	AR32	VSS
AR1	SPI_0_SCLK	AR33	VSS
AR2	SPI_1_SS_N[2]	AR34	VSS
AR3	SPI_1_SS_N[1]	AR35	VDD
AR4	SPI_1_SS_N[0]	AR36	VSS
AR37	VDD	AT32	PCIE_RX_P[0]
AT1	SPI_1_D[6]	AT33	VSS
AT2	SPI_1_D[7]	AT34	VDD
AT3	SPI_1_D[4]	AT35	VSS
AT4	SPI_1_D[5]	AT36	VDD
AT5	SPI_1_D[3]	AT37	VSS
AT6	SDIO_DAT[2]	AU1	VSS
AT7	SDIO_CRD_WR_PROT	AU2	VSS

Table 5-2. MLSoC SM1 Pin and Signal Names (continued)

Pin Name	Signal Name	Pin Name	Signal Name
AT8	JTAG_TCK	AU3	SPI_1_D[2]
AT9	VSS	AU4	SPI_1_D[1]
AT10	ETH_3_RX_P	AU5	VSS
AT11	VSS	AU6	SPI_1_D[0]
AT12	ETH_2_RX_P	AU7	SDIO_ENA
AT13	VSS	AU8	JTAG_TMS
AT14	ETH_1_RX_P	AU9	VSS
AT15	VSS	AU10	ETH_3_RX_M
AT16	ETH_0_RX_P	AU11	VSS
AT17	VSS	AU12	ETH_2_RX_M
AT18	PCIE_RX_P[7]	AU13	VSS
AT19	VSS	AU14	ETH_1_RX_M
AT20	PCIE_RX_P[6]	AU15	VSS
AT21	VSS	AU16	ETH_0_RX_M
AT22	PCIE_RX_P[5]	AU17	VSS
AT23	VSS	AU18	PCIE_RX_N[7]
AT24	PCIE_RX_P[4]	AU19	VSS
AT25	VSS	AU20	PCIE_RX_N[6]
AT26	PCIE_RX_P[3]	AU21	VSS
AT27	VSS	AU22	PCIE_RX_N[5]
AT28	PCIE_RX_P[2]	AU23	VSS
AT29	VSS	AU24	PCIE_RX_N[4]
AT30	PCIE_RX_P[1]	AU25	VSS
AT31	VSS	AU26	PCIE_RX_N[3]
AU27	VSS	AU29	VSS
AU28	PCIE_RX_N[2]	AU30	PCIE_RX_N[1]
AU31	VSS	AU35	VDD
AU32	PCIE_RX_N[0]	AU36	VSS
AU33	VSS	AU37	VDD
AU34	VSS	-	-

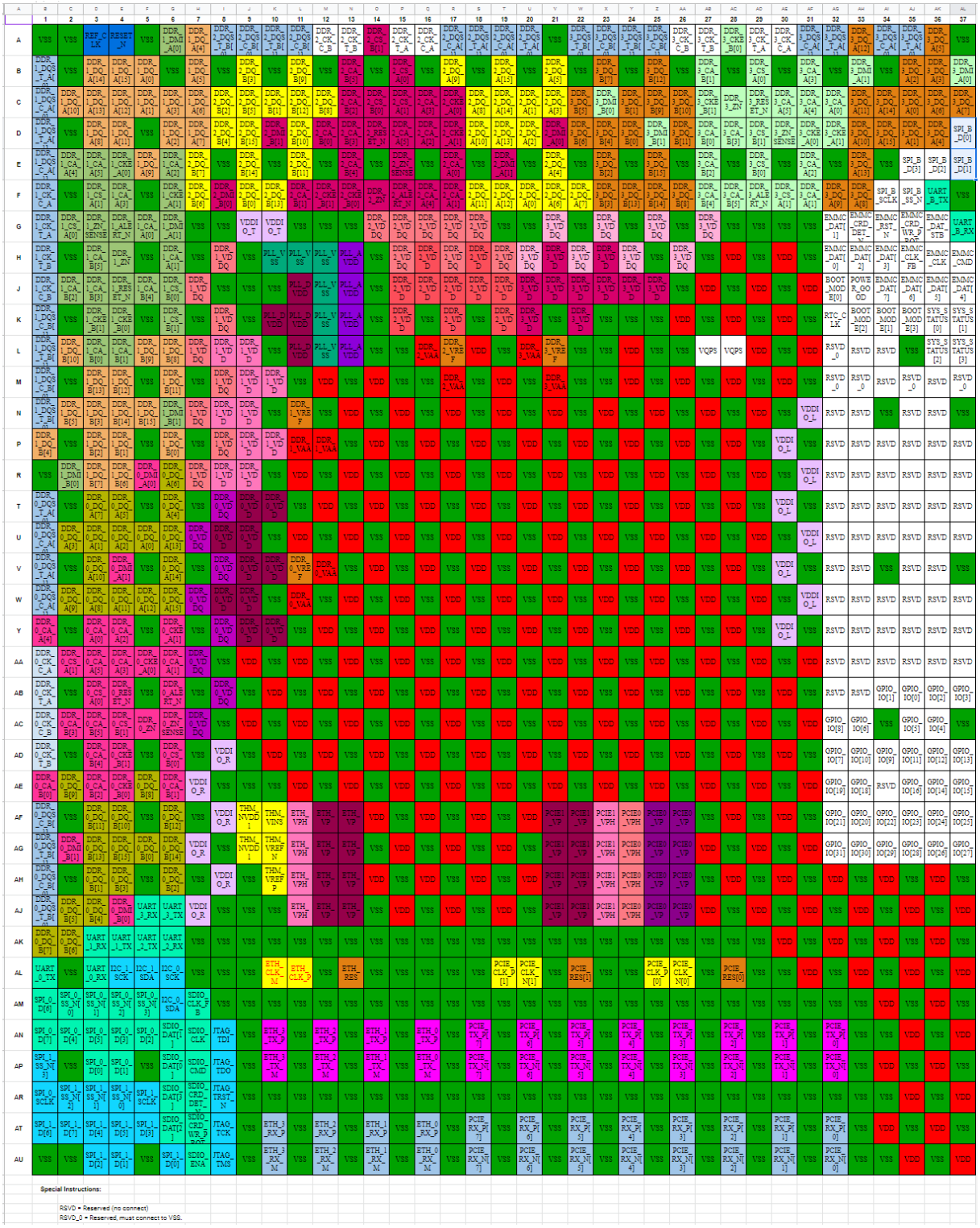


Figure 5-1. MLSoC SM1 Signal and Pin Names Map

Chapter 6
Electrical Specifications

This chapter describes the power supply on the MLSoC SM1, including nominal voltages and tolerance ranges.

6.1 Power Supply

"Table 6-1." shows the nominal voltages and tolerance ranges for various power supplies.

Table 6-1. Nominal Voltages, Power Supplies, and Tolerance Ranges

Ball Name	Nominal Voltage	Supply Name	Tolerance/Range	Special Requirement
VDD	0.84V	VDD core supply	- 3% / + 5%	Max power = 25W
PLL_AVDD	1.8V	PLL Analog Voltage Supply	(± 5%)	Max voltage ripple 50mV peak-to-peak
PLL_DVDD	0.84V	PLL Digital Voltage Supply	Same as VDD	N/A
VDDIO_L	1.8V	IO supply	(± 5%)	N/A
VDDIO_R	1.8V	IO supply	(± 5%)	N/A
VQPS	1.8V	EFuse Programming Voltage supply	(± 5%)	N/A
PCIE1_VP	0.84V	PCIE Low Voltage Supply	Same as VDD	N/A
PCIE1_VPH	1.8V	PCIE High Voltage Supply	(± 5%)	Max voltage ripple 50mV peak-to-peak
PCIE0_VP	0.84V	PCIE Low Voltage Supply	Same as VDD	N/A
PCIE0_VPH	1.8V	PCIE High Voltage Supply	(± 5%)	Max voltage ripple 50mV peak-to-peak
ETH_VPH	1.8V	Ethernet High Voltage Supply	(± 5%)	Max voltage ripple 50mV peak-to-peak
ETH_VP	0.84V	Ethernet Low Voltage Supply	Same as VDD	N/A
THM_NVDD1	1.8V	Thermal Monitor power supply	(± 5%)	N/A
DDR_0_VAA	1.8V	DRAM LPDDR4 PLL Supply Interface 0	(± 5%)	Max voltage ripple 50mV peak-to-peak
DDR_0_VDD	0.84V	DRAM LPDDR4 Logic Supply Interface 0	Same as VDD	N/A
DDR_0_VDDQ	1.11V	DRAM LPDDR4 IO Supply Interface 0	(Min: 1.06V, Max: 1.17V)	N/A
DDR_1_VAA	1.8V	DRAM LPDDR4 PLL Supply Interface 1	(± 5%)	Max voltage ripple 50mV peak-to-peak
DDR_1_VDD	0.84V	DRAM LPDDR4 Logic Supply Interface 1	Same as VDD	N/A
DDR_1_VDDQ	1.11V	DRAM LPDDR4 IO Supply Interface 1	(Min: 1.06V, Max: 1.17V)	N/A
DDR_2_VAA	1.8V	DRAM LPDDR4 PLL Supply Interface 2	(± 5%)	Max voltage ripple 50mV peak-to-peak
DDR_2_VDD	0.84V	DRAM LPDDR4 Logic Supply interface 2	Same as VDD	N/A

Table 6-1. Nominal Voltages, Power Supplies, and Tolerance Ranges (continued)

Ball Name	Nominal Voltage	Supply Name	Tolerance/Range	Special Requirement
DDR_2_VDDQ	1.11V	DRAM LPDDR4 IO Supply Interface 2	(Min: 1.06V, Max: 1.17V)	N/A
DDR_3_VAA	1.8V	DRAM LPDDR4 PLL Supply Interface 3	(± 5%)	Max voltage ripple 50mV peak-to-peak
DDR_3_VDD	0.84V	DRAM LPDDR4 Logic Supply Interface 3	Same as VDD	N/A
DDR_3_VDDQ	1.11V	DRAM LPDDR4 IO Supply Interface 3	(Min: 1.06V, Max: 1.17V)	N/A

6.2 Power Rails

When executing an AI/ML model, there can be sudden increases in the current drawn by the MLSoC which can affect its stability and performance. Therefore, it is necessary to carefully design the power rails to maintain a steady state of the power supply.

"Figure 6-1." shows an overview of the MLSoC power rails.

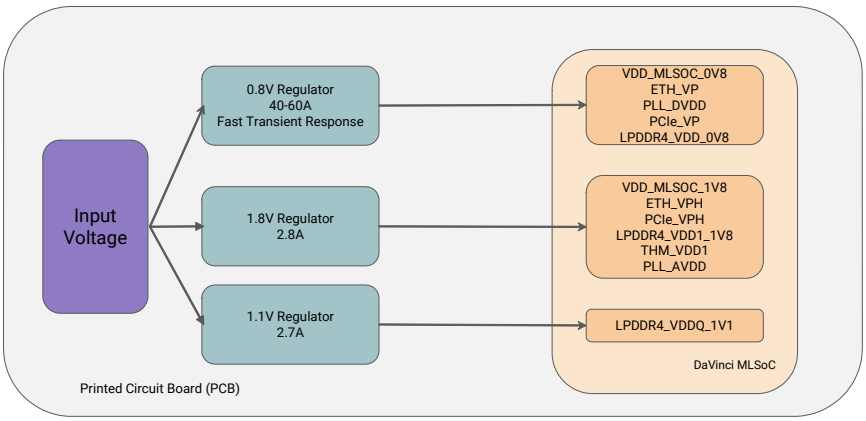


Figure 6-1. MLSoC Power Rails Overview

6.2.1 Design Considerations

To maintain optimal performance of the SiMa.ai MLSoC device operating at 50 TOPS with power consumption under 20 watts in a steady state, the key considerations are listed below.

- A core voltage regulator (0.84V) with excellent transient current response is required to minimize the voltage rail droop.
- Depending on the type and complexity of the AI/ML model, a voltage regulator supporting a minimum of 40A at 0.84V is necessary, while 60A at 0.84V is desirable to ensure stability and performance.
- Regulators with lower current ratings may be suitable for less demanding models. Key considerations include excellent transient response, high efficiency, and effective thermal management to prevent voltage rail droop and ensure reliable operation.

NOTE The design considerations listed above are for the MLSoC only and not for the other components including the LPDDR Memory devices, FLASH, eMMC, and so forth.

Chapter 7
MLSoC Packaging Information

This chapter provides the packaging information for MLSoC SM1.

7.1 1369-ball FCBGA

The MLSoC is available in 1369-ball high-performance BGA (FCBGA), 31mm × 31mm, 0.8mm pitch. "Figure 7-1." shows the top and side view of the package.

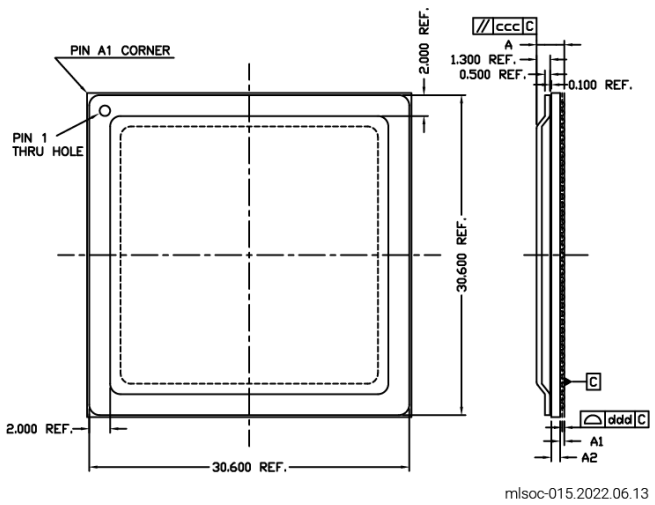


Figure 7-1. MLSoC Top and Side View

"Figure 7-2." shows the bottom view of the package.

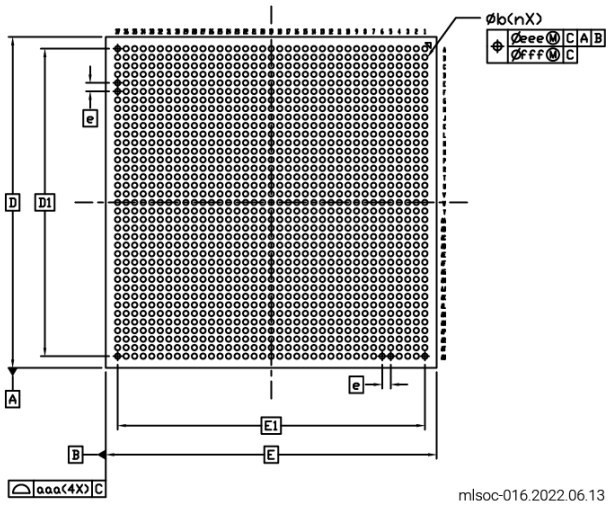


Figure 7-2. MLSoC Bottom View

"Table 7-1." shows the MLSoC package dimensions.

Table 7-1. MLSoC Package Dimensions

Parameter	Symbol	Common Dimensions (All dimensions in mm)		
		Min	Nom	Max
Total thickness	A	2.508	2.648	2.788
Stand-off	A1	0.300		0.500
Substrate thickness	A2	0.848 (REF)		
Body size	D/E	31.000 (BSC)		
Ball diameter		0.500		
Ball width	b	0.400	-	0.600
Ball pitch	e	0.800 (BSC)		
Ball count	n	1369		
Edge ball center to center	D1/E1	28.800 (BSC)		
Package edge tolerance	aaa	0.200		
Top parallelism	ccc	0.350		
Coplanarity	ddd	0.200		
Ball offset (package)	eee	0.200		
Ball offset	fff	0.080		

7.2 Package Thermal Resistance

Table 7-2. MLSoC Package Thermal Resistance

Ambient Temperature: 25° C, Power: 50 Watts		
$^{\theta}$JA (° C/W)	$^{\theta}$JC (° C/W)	$^{\theta}$JB (° C/W)
4.05	0.108	0.504

Chapter 8
MLSoC Ordering Information

This chapter describes the two options available for ordering the SiMa.ai MLSoC SM1 device.

8.1 Commercial / Industrial Temperature Range

The MLSoC SM1 device is available in two different temperature ranges:

- Commercial temperature (0°C to 70°C) – SM1-200A-C0AA0
- Industrial temperature (-40°C to 85°C) – SM1-200A-I0AA0

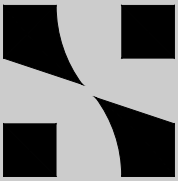
Table 8-1. Commercial and Industrial Grade Operating Range

Parameter	Commercial Grade Req. -> Ambient 0° to 70° C		Industrial Grade Req. -> Ambient —40° to 85° C
MaxTj	85° C	105° C	115° C
Typical voltage supplies (± 5% for Vmax/Vmin)	Core – 0.84V; I/Os – 1.1V, 1.8V	Core – 0.84V; I/Os– 1.1V, 1.8V	Core – 0.84V; I/Os – 1.1V, 1.8V
Operating frequency	MLA -1 GHz NOC -1 GHz APU -1.15 GHz	MLA -800 MHz NOC -800 MHz APU -1 G Hz	MLA -800 MHz NOC -800 MHz APU -1 GHz
MLA TOPS	50	40	40

Chapter 9
Support

If you have any questions, please contact support@sima.ai .

Document No: 001-HW-24, Rev. D



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