MLSoC™ Dual M.2 Board Hardware Reference Manual

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Revision History

This document describes the SiMa.ai MLSoC Dual M.2 Board. The table below provides a history of changes made to this document.

Date	Version	Description
August 11, 2023	A	Initial release.
November 7, 2023	B	Updated per technical and editorial review.

About this Document

SiMa.ai's Machine Learning System on Chip (MLSoC) delivers high-performance, effortless machine learning inference for embedded edge applications. Built on 16nm technology, the MLSoC's processing system consists of a computer vision processor, coupled with dedicated Machine Learning Acceleration (MLA) and high-performance application processors. Surrounding various processors are memory interfaces, communication interfaces, and system management, all connected via a Network on Chip (NoC).
The SiMa.ai MLA Intellectual Property (IP) is the core of the SiMa.ai MLSoC which provides a platform for accelerating next generation machine learning applications.

NOTE! Signal direction and Input/Output (IO) types mentioned in the [illegible] are defined with respect to the MLSoC device.

Purpose and Scope

This document provides high-level design and hardware reference information for the MLSoC Dual M.2 Board using the SiMa.ai MLSoC device.
This document describes the MLSoC Dual M.2 Board including its implementation, block-level functional description of each interface, power requirements, reset sequence, and the Printed Circuit Board (PCB) characteristics.
It covers the following topics:

- General safety guidelines and precautions
- Board overview
  - Configuration details
  - Architecture and block level functional description of each interface
- Peripheral Component Interconnect Express (PCIe) implementation
- Power requirements
- Board specifications
- Clock requirements
- Reset sequence
- Operation and maintenance
- Signal Integrity (SI) and Power Integrity (PI) thermal analysis
- Environmental and compliance
- Technical support

Intended Audience

This document is intended for hardware/system engineers who are interested in deploying the SiMa.ai MLSoC Dual M.2 Board into their design. It also serves as a reference for the designers who want to design their own PCB with SiMa's MLSoC chip. An advanced knowl-

edge of high-speed circuit/PCB design, memory interfaces, and familiarity with various Ethernet, PCIe-based designs, etcetera (etc.), is required.

Known Issues

Issue: There are 32 GPIOs on the SiMa.ai MLSoC device. However, only 31 of them are available for use.
Resolution: Not applicable.

Reference Documentation

These documents provide additional information in understanding the SiMA.ai products:

- MLSoC device, also known as the chip
- Palette software, also known as the SDK (Software Development Kit)

Table ii-1. SiMa.ai Documents

Name	Description
MLSoC™ SM1 Datasheet	Provides product overview and architectural overview of the MLSoC SM1 device. In addition, it provides pinout information, electrical specifications, thermal specifications, packaging information, and ordering information.
MLSoC™ Evaluation Board Hardware Reference Manual	Serves as a reference for the designers who want to design their own PCB/board with SiMa.ai's MLSoC chip.
MLSoC™ Dual M.2 Board Product Brief	Introduces the key features of this product, including the interfaces and functional block diagram of the Dual M.2 Board.
MLSoC™ PCIe Half-height, Half-length Production Board Product Brief	Introduces the key features of this product, including the interfaces and functional block diagram of the MLSoC PCIe Half-height Half-length Board (PCIe HHHL Board).
MLSoC™ PCIe Half-height, Half-length Production Board Hardware Reference Manual	Provides an overview of SiMa.ai's MLSoC PCIe Half-height Half-length Board including details on safety guidelines, clock requirements, power requirements, system reset, operation and maintenance, certification data, and so on.
MLSoC™ (Machine Learning System on Chip) Product Brief	Provides MLSoC highlights, overview and architecture features. It covers basic power on, reset, and clock test procedures, SPI configuration, and board interfaces.
MLSoC™ Evaluation Board Product Brief	Introduces key features of the MLSoC device. In addition, it provides a functional block diagram that shows all the major blocks of the MLSoC Evaluation Board.
Palette™ Developer User Guide	Describes the SiMa.ai's Palette software platform including how to compile, build, and deploy real-time applications, in conjunction with the MLSoC Evaluation Board. Additionally, the developers can debug, evaluate performance, and fine-tune applications.
Palette™ Product Brief	Introduces the SiMa.ai's Palette software platform which is designed for complete ML stack application development.

Table ii-2. Internal/External Document URL Links

URL Link	Description
1. https://developer.sima.ai/	Developer Zone for SiMa.ai customers. Request access for the latest software download and documentation by sending email to: **developer.mlsoc@sima.ai**

List of Acronyms

The following acronyms are used in this document.

Table ii-3. Acronyms

Acronym	Description
DFM	Design for Manufacturability
DFT	Design for Testability
DRAM	Dynamic Random-Access Memory
EMI	Electromagnetic Interference
eMMC	Embedded MultiMediaCard
FEXT	Far End Cross Talk
ESD	Electrostatic discharge
HHHL	Half Height Half Length
Gbps	Giga Bits Per Second
GPIO	General Purpose Input Output
I2C	Inter Integrated Circuit
IBIS	IO Buffer Information Specification
IC	Integrated Circuit
JTAG	Joint Test Action Group
LED	Light Emitting Diode
MB	Mega Byte
MHz	Mega Hertz
MLSoC	Machine Learning System on Chip
mm	Millimeter
MDIO	Management Data Input/Output
MIPI	Mobile Industry Processor Interface

Table ii-3. Acronyms (continued)

Acronym	Description
NEXT	Near End Cross Talk
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PCIe HHHL	Peripheral Component Interconnect express Half Height Half Length Board, also known as industry standard PCIe Low Profile Board.
PD	Power Delivery
PI	Power Integrity
PMIC	Power Management Integrated Circuit
POS	Position
QSPI	Quad Serial Peripheral Interface
R/A	Right Angled
RoHS	Restriction of Hazardous Substances
S	Scattering
SBC	Single Board Computer
SD	Secure Digital
SGMII	Serial Gigabit Media-Independent Interface
SI	Signal Integrity
SMD	Surface Mount Device
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
TBD	To Be Determined
UART	Universal asynchronous receiver-transmitter
USB	Universal Serial Bus

Chapter 1
General Safety Guidelines and Precautions

This chapter provides general safety guidelines and precautions when handling the MLSoC Dual M.2 Board. These guidelines and precautions must be followed when handling the MLSoC Dual M.2 Board and working with electricity to avoid any damage to the board and personal injury.

CAUTION! Follow these safety precautions and warnings. Failure to comply may result in damage to the board.

- Use proper ESD grounding techniques when handling the board.
- Wear an antistatic wrist strap and use an ESD-protected mat.
- Do not touch the board in power on state.
- Store the board in an antistatic bag before placing it on any surface.
- Handle the module from the edges and avoid touching any of the onboard ICs/components.
- Do not connect any higher I/O voltage level signals than specified in the SM1 Datasheet.
- Use the appropriate power supply that is supplied with the module.
- After power on, make sure all the power indication LEDs are lit.

WARNING! Use the following safety precautions. Failure to comply may result in damage to the board and/or result in personal injury.

- Boards are not conformal coated and can get damaged due to water or any other conductive liquids. Keep water and other conductive liquids away from the MLSoC Dual M.2 Board.

Chapter 2
Overview

The MLSoC Dual M.2 Board has been designed to meet the next generation edge applications and includes the following:

- PCIe Gen 4.0 x8 interface, I2C, SPI-8, 1G Ethernet, JTAG, UART, LPDDR4, and GPIO interfaces.
- The board's form factor has the board edge fingers for the PCIe x8 interface of 150 pins in the south edge of the PCB (Printed Circuit Board).

Figure 2-1. shows the top view of the MLSoC Dual M.2 Board.

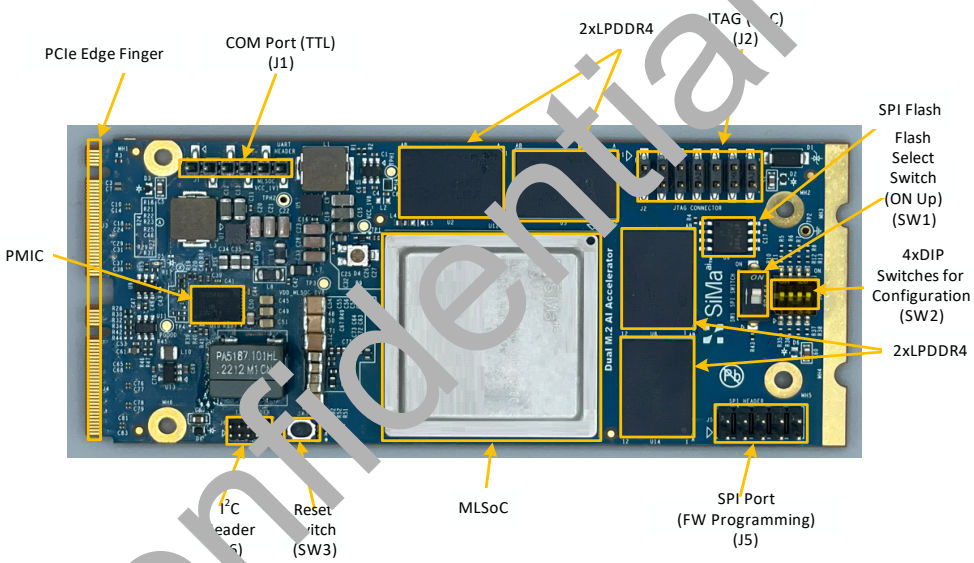

Figure 2-1. MLSoC Dual M.2 Board Top View

2.1 Architecture

The MLSoC Dual M.2 Board was designed using the MLSoC device. Its high-level architecture functional block diagram is shown in **Figure 2-2.**

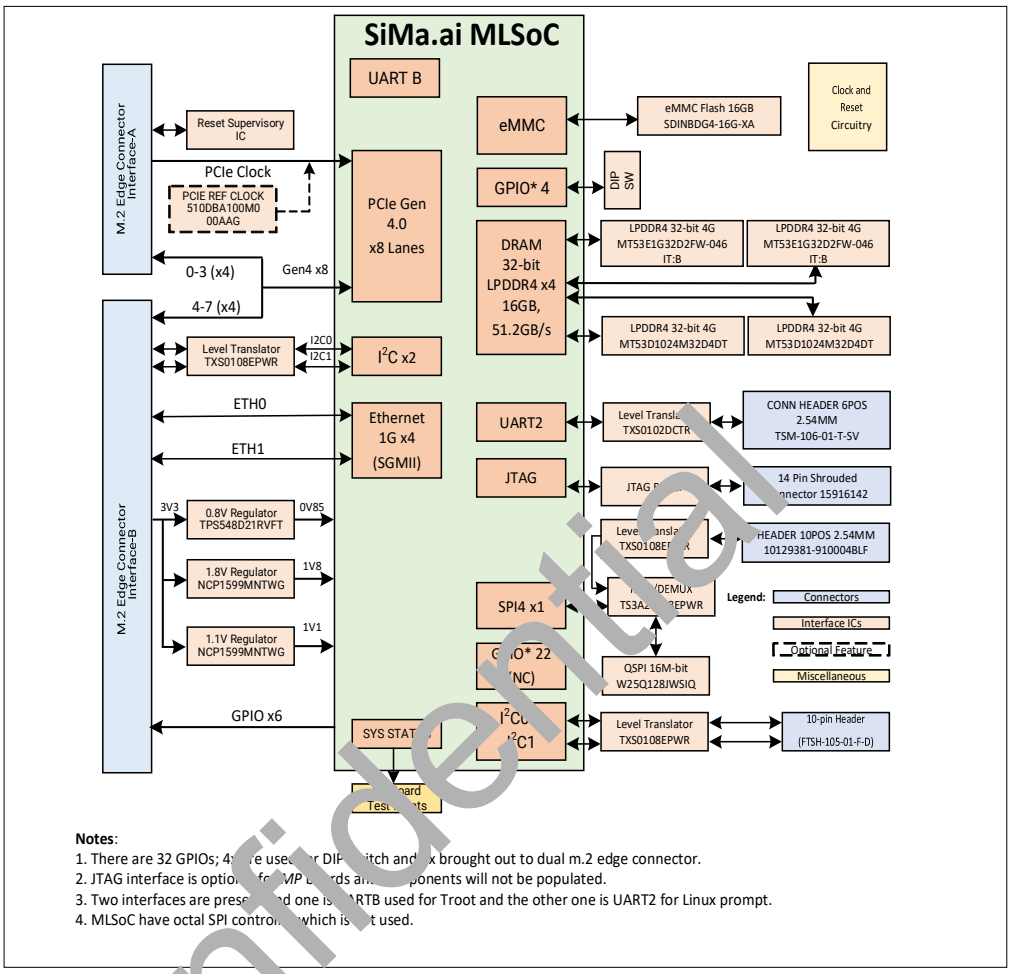

Figure 2-2. MLSoC Dual M.2 Board Functional Block Diagram

CAUTION! Do not use the board for any purpose other than its intended use.

2.2 Dual M.2 Board Features

- 1x of PCIe Gen 4.0 x8 link Interface with standard board edge connector in Dual M.2 Board configuration.
- 4x 4GB 32Bit LPDDR4 DRAM Interface
- 1x 16GB eMMC Flash Memory Interface
- 1x 128Mbit QSPI NOR Flash Interface
- 2x SGMII Interface for 1 Gbps Ethernet PHY
- 2x I^2C Interfaces with header
- 1x JTAG Interface (optional)
- 1x Debug UART for tRoot
- 1x Debug UART for Linux

2.2.1 Board Dimensions (Form Factor)

- Form Factor: 110mm (L) x 46mm (H) Standard Dual M.2 Board
- Height restriction: 1.62mm on top layer and 1.9mm on bottom layer. Height keep out defines the SMT component and does not include the heat sink or thermal materials

2.2.2 Board Operating Temperature

- – 40°C to +85°C (Industrial grade)
- 0°C to 70°C (commercial grade)

2.3 MLSoC Dual M.2 Board Interface

2.3.1 MLSoC Architecture

SiMa.ai MLSoC is the main processor for MLSoC Dual M.2 Board. Following are the details of the MLSoC Dual M.2 Board chip set:

- Part Number:
  - SM1-200A-C0AA0 (Commercial 50 TOPS) 1 GHz clock speed
  - SM1-200A-I0AA0 (Industrial 40 TOPS) 816 MHz clock speed
- DRAM Controller: 4x 32-bit DRAM
- PCIe blocks: 1x PCIe Gen 4.0 x8 lanes
- SGMII block for Ethernet PHY: 2x 1Gbps
- Total Number of IOs: 32 GPIOs
- Package: 1369-ball high-performance Flip Chip Ball Grid Array (FCBGA) package
- MLSoC temperature grade:
  - – 40°C to +85°C (Industrial)
  - 0°C to 70°C (Commercial)

2.3.2 MLSoC Power Requirements

Table 2-1. MLSoC Power Requirements

Power Rail	Typical Voltage	Tolerance	Selected Regulator Max Current Output (A)
MLSoC_Core	0.85V	–7% to +10%	40
VDDIO	1.8V	–7% to +10%	2.4
VDDQ	1.1V	–7% to +10%	2.5

2.3.3 Power Up Sequencing

The MLSoC and memory interface supply voltages are powered up by separate regulators than the ones used for generating the power supply for other on-board circuitries.

Figure 2-3. shows the preliminary implementation of the power sequencing of the MLSoC Dual M.2 Board.

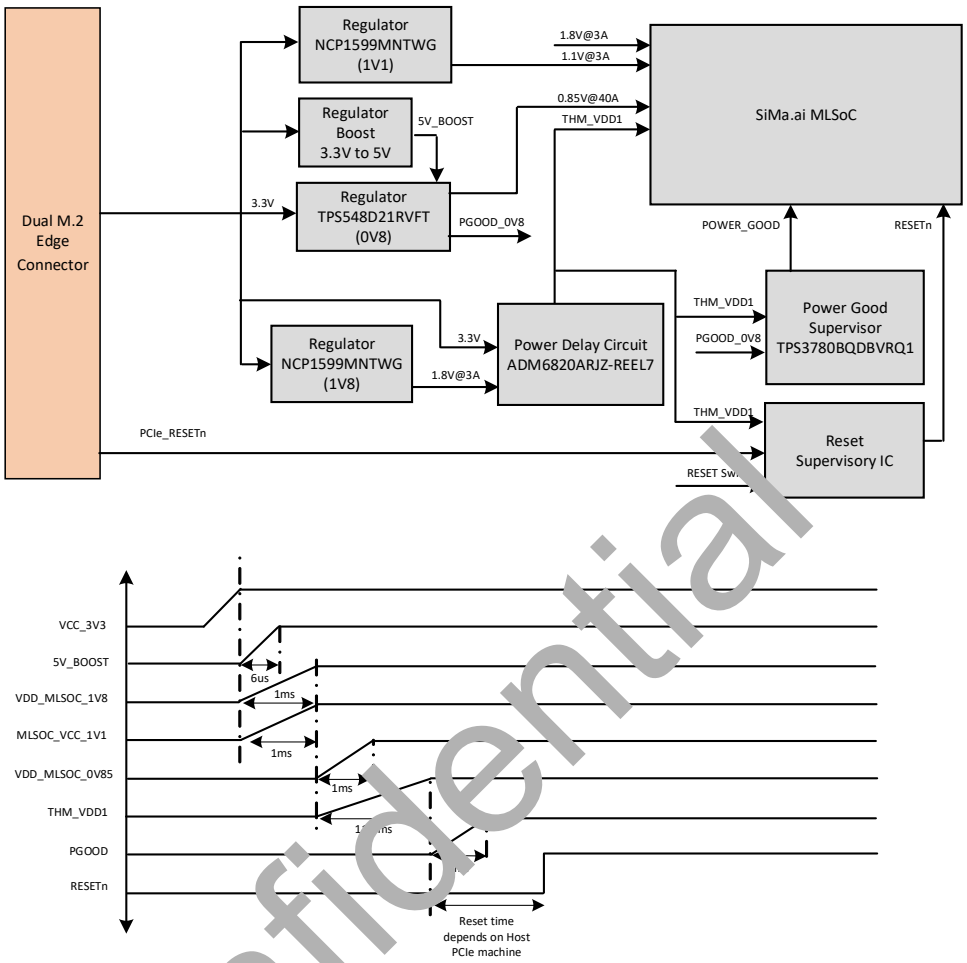

Figure 2-3. Dual M.2 Board Power Up Sequencing Implementation

The values which are given in “ms” are the soft-start time for each regulator. The current values in Amps are the maximum current which can be sourced by the regulator, not the actual power requirement. More details on power circuitry for the entire board are provided in **Chapter**

2.4 MLSoC Interfaces

This section contains detailed information about all the interface design enabled on the MLSoC Dual M.2 Board.

2.4.1 Dual M.2 Board Specifications

Table 2-2. Dual M.2 Board Specifications

Item	Name	Description
1	Processor/SoC	SiMa.ai MLSoC
2	LPDDR4	4x 4GB SDRAM – LPDDR4
3	eMMC	16GB eMMC 5.1 industrial NAND
4	I^2C	2x I^2C interface
5	SGMII	2x SGMII for two 1G Ethernet PHYs
6	UART	2x UART interfaces
7	JTAG	1 JTAG (optional)
8	Quad SPI	1 x Quad SPI interfaces
9	PCIe Gen 4.0	PCIe Gen 4.0 x8 Interface
10	Cooling	Conduction cooled
11	Operating Temperature	0°C to 70°C (commercial) – 40°C to +85°C (Industrial)

2.4.2 LPDDR4 Interface (32-bit)

- 4x 32-bit LPDDR4 memory controllers are present in the MLSoC chip/device.
- DRAM addressing up to 16GB is supported by the MLSoC.
- Each memory controller supports a maximum of 933MHz for the clock frequency.
- The voltage requirement for each memory controller is as follows:
  - DDR_VDD = 0.85V
  - DDR_VDDQ = 1.1V
  - DDR_VAA = 1.8V
  - VREF voltage to be supplied internally
- The ZN pin for connecting the calibration resistor of each memory controller must be pulled to ground through an external 120-ohm ±1% calibration resistor.
- The ALERT_N signal is an output signal from the memory controller. So this signal for each controller needs to be connected to a test point on the board.
- 4x 32-bit LPDDR4 chips with P/N MT53E1G32D2FW-046 IT:B from Micron are mounted on the MLSoC Dual M.2 Board.

- Each LPDDR4 chip is of 4GB density.
- Supports four 32-bit LPDDR4 memory controllers and PHY interfaces operating at up to 3733 million transfer/s.
- Voltage requirement of each LPDDR4 IC is as follows:
  - VDD1 = 1.8V
  - VDD2 = 1.1V
  - VDDQ = 1.1V
- The LPDDR4 device requires voltage sequencing. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ. Also, VDD1 must be greater than VDD2 and VDD2 must be greater than VDDQ – 200mV.
- Since separate controllers are present in the MLSoC, command/address, control and data signals connected one to one from the MLSoC to LPDDR4 memory devices.
- The ZQ calibration pins of the DDR are connected to VDDQ through 240-ohm ±1% resistor.
- The Zn and Zn_S pins of the MLSoC are shorted and connected to ground through a single 120-ohm ±1% resistor.
- The LPDDR4 memory device command or the address On Die Termination (ODT) control signals, ODT_CA_A, ODT_CA_B are pulled to VDD2 for enabling on-die termination.
- The power requirement for each memory controller in the MLSoC is shown in **Table 2-3.**

Table 2-3. LPDDR4 Voltage Requirement Per Memory Device

Item No.	Power Rail	Voltage (V)	Tolerance	Current Requirement (A)
1	VDD1	1.8	±100mV	0.033
2	VDD2	1.1	±40mV	1.012
3	VDDQ	1.1	±40mV	0.0105

Figure 2-4. shows the bock level connection between MLSoC and LPDDR4.

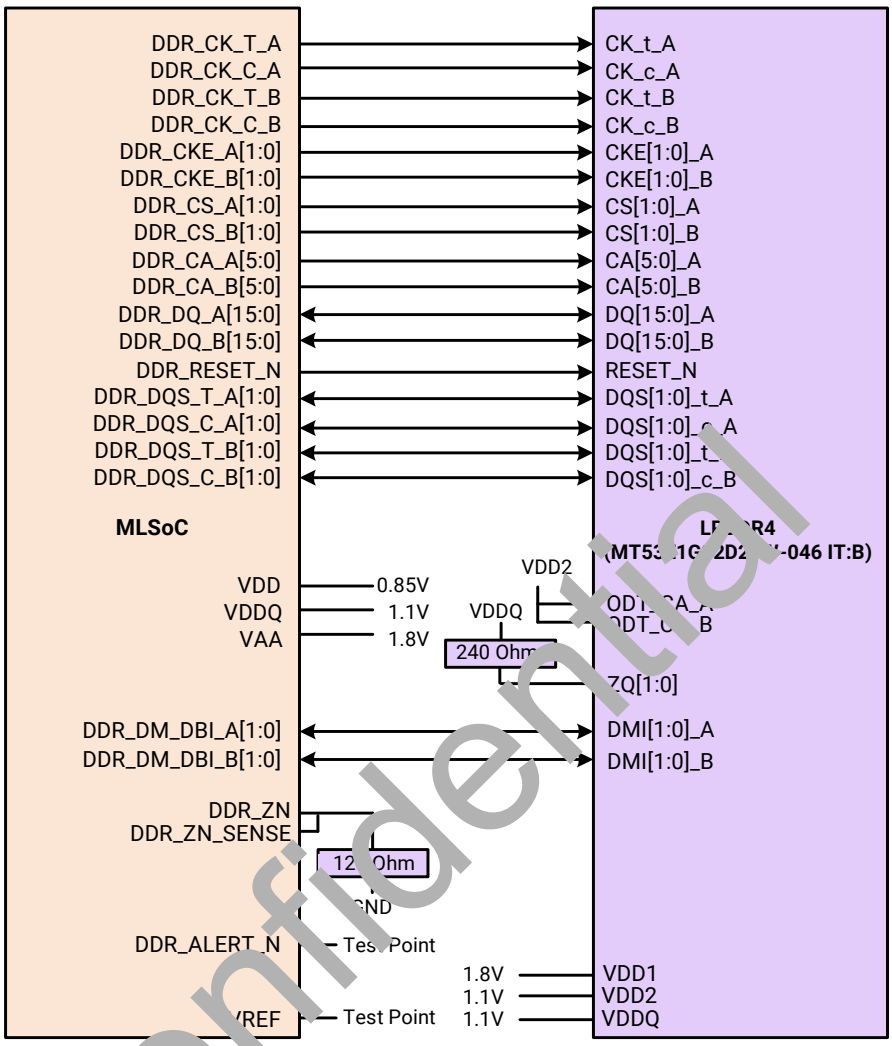

Figure 2-4. MLSoC to LPDDR4 Interface

The MLSoC four DDR controller instances are connected to four LPDDR4 memory device instances.

Table 2-4. LPDDR4 Interface Signal Pin-outs

Interface Signals		IO Description
MLSoC	**LPDDR4**	
DM_RST_N	RESET N	OUTPUT
DM_CSA[1:0]	CS[1:0]_A	OUTPUT
DM_CKEA[1:0]	CKE[1:0] A	OUTPUT
DM_CKTA	CK_t_A	OUTPUT
DM_CKCA	CK_c_A	OUTPUT
DM_CAA[5:0]	CA[5:0]_A	OUTPUT
DM_DQA[15:0]	DQ[15:0]_A	Bi-directional
DM_DMIA[1:0]	DMI[1:0]_A	Bi-directional
DM_DQSTA[1:0]	DQS[1:0]_t_A	Bi-direction
DM_DQSCA[1:0]	DQS[1:0]_c_A	Bi-direct
DM_CSB[1:0]	CS[1:0]_B	OUTPUT
DM_CKEB[1:0]	CKE[1:0]_B	TPUT
DM_CKTB	CK_t_B	UT
DM_CKCB	CK c_B	TPUT
DM_CAB[5:0]	CA[5:0]_	OUTPUT
DM_DQB[15:0]	DQ[ ]_A	Bi-directional
DM_DMIB[1:0]	[1:0]_	Bi-directional
DM_DQSTB[1:0]	S[1:0]_t_B	Bi-directional
DM_DQSCB[1:0]	DQS[1:0]_c_B	Bi-directional

2.4.3 MLSoC eMMC Interface

- The eMMC controller in the MLSoC is compliant with the eMMC 5.1 specification and earlier versions.
- The MLSoC supports clock speed up to 52MHz.
- A 16GB eMMC Flash with P/N SDINBDG4-16G-XI1 is used on the Dual M.2 Board.
- This is an eMMC 5.1 with HS400 interface and eMMC Flash (NAND type memory).
- The sequential read speed of this flash is 300MBps and the write speed is 80MBps.
- The voltage requirement for the eMMC flash IC is as follows:
  - Core Voltage (VC) = 3.3V
  - IO Voltage (VCCQ) = 1.8V
- The eMMC flash device supports variable clock frequencies of 0-20MHz, 0-26MHz (Default), 0-52MHz (High-speed), 0-200MHz Single Data Rate (HS200), 0-200MHz Double Data Rate (HS400).
- The mechanical design of the eMMC device is Joint Electron Device Engineering Council (JEDEC) compliant.
- The eMMC Card detect pin EMMC_CRD_DET_N is pulled low to indicate that an eMMC flash is connected.
- The eMMC write protect pin EMMC_CRD_WP_PROT is used to configure eMMC as read only. Both pull-up and pull-down options are provided, and by default, this pin should be pulled high.

Table 2-5 Power Requirement for eMMC Flash IC

Item No.	Power Rail	Voltage (V)	Tolerance	Current Requirement (A)
1	VCC	3.3	± 300mV	0.23
2	VCCQ	1.8	± 150mV	.295

Figure 2-5. represents the block-level connection between the MLSoC and the eMMC flash.

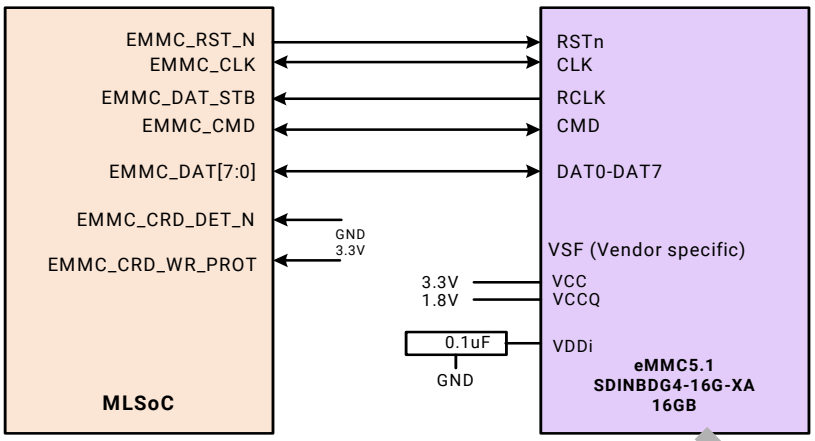

Figure 2-5. MLSoC eMMC Interface

See **Table 2-6.** for the MLSoC eMMC interface pin-out.

Table 2-6. MLSoC eMMC Interface Pin-out

Interface Signals		Signal Description
MLSoC	MMC	
EMMC_CLK	CLK	OUTPUT
EMMC_CLK_FB	CLK	INPUT
EMMC_DAT_STB	M_STB	INPUT
EMMC_CMD	CMD	Bi-directional
EMMC_RST_N	EM_RST	OUTPUT
EMMC_DAT[7:0]	DAT0-DAT7	Bi-directional
EMMC_CRD_DET_N (Card detect)	NA	INPUT
EMMC_CRD_WR_PROT (Write protect)	NA	INPUT

2.4.4 MLSoC I2C Interface

- Two IC controllers are present in the MLSoC.
- The I2C controllers' clock frequency is up to 400 KHz for fast mode as per standard.
- All the I2C SCL and SDA lines are provided with 2.2K-ohm pull-up resistors.
- The I2C0 bus signals are connected to both the 10-pin header J6 as well as one of the Dual M.2 connectors J3. The I2C1 bus signals are connected to both the 10-pin header J6 as well as one of the Dual M.2 connectors J4.

Figure 2-6. shows the block level connection between I2C interfaces of the MLSoC.

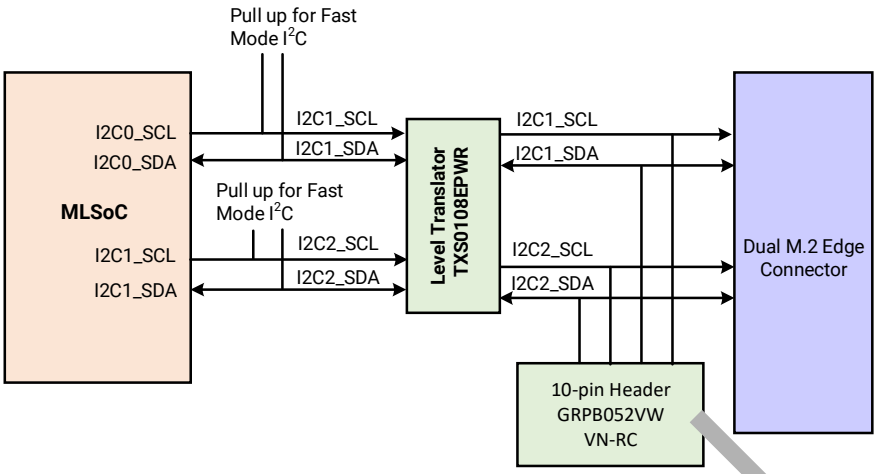

Figure 2-6. MLSoC I2C Interface

Table 2-7. shows the Dual M.2 Board pin-out.

Table 2-7. I2C Dual M.2 Board Pin-out

I2C Interface Signal	Level Translator	I2C Top Pin Header Pin	Dual M.2 Edge Connector Pin	IO Standards
I2C0_SCL	A1/B1	J6.5	J3.40 and J4.69	Output
I2C0_SDA	A2/B2	J6.6	J3.42 and J4.67	Bi-directional
I2C1_SCL	A3/B3	J6.1	J4.55	Output
I2C1_SDA	A4/B4	J6.2	J4.53	Bi-directional
3.3V power	NA	J6.9 and J6.10	X	Power
GND	NA	J6.3 and J6.7	X	Power
NC	NA	NA	X	No Connect

2.4.5 Ethernet MAC Interface

- Four 1Gigabit Ethernet controllers are present in the MLSoC device.
- The MLSoC Media Access Control (MAC) supports an SGMII Interface. With the Dual M.2 Board, the SGMII interface from the MLSoC is directly brought out and connected to the Dual M.2 edge connector.
- The voltage requirement for the MLSoC Ethernet SGMII is as follows:
  - ETH_VP = 0.85V
  - ETH_VPH = 1.8V
- The SGMII MAC signals run at a 1.8V IO level
- A 156.25MHz Low Voltage Differential Signaling (LVDS) clock with P/N ASEMPLV-156.250MHz-LR-T is connected to the Ethernet MAC reference clock pins.
- The Ethernet RESREF pin of the MAC is tied to ground via a 2.0-ohm ±1% resistor on the board.

Table 2-8. describes the power requirements for the MLSoC Ethernet PHY.

Table 2-8. Power Requirements for MLSoC Ethernet PHY

Item No.	Power Rail	Voltage (V)	Tolerance	Current Requirement (A)
1	ETH_VPH	1.8	± 125mV	0.086
2	ETH_VP	0.85	± 110mV	0.05

Figure 2-7. shows the block diagram which represents the block level connections between the MLSoC and the Dual M.2 edge connector.

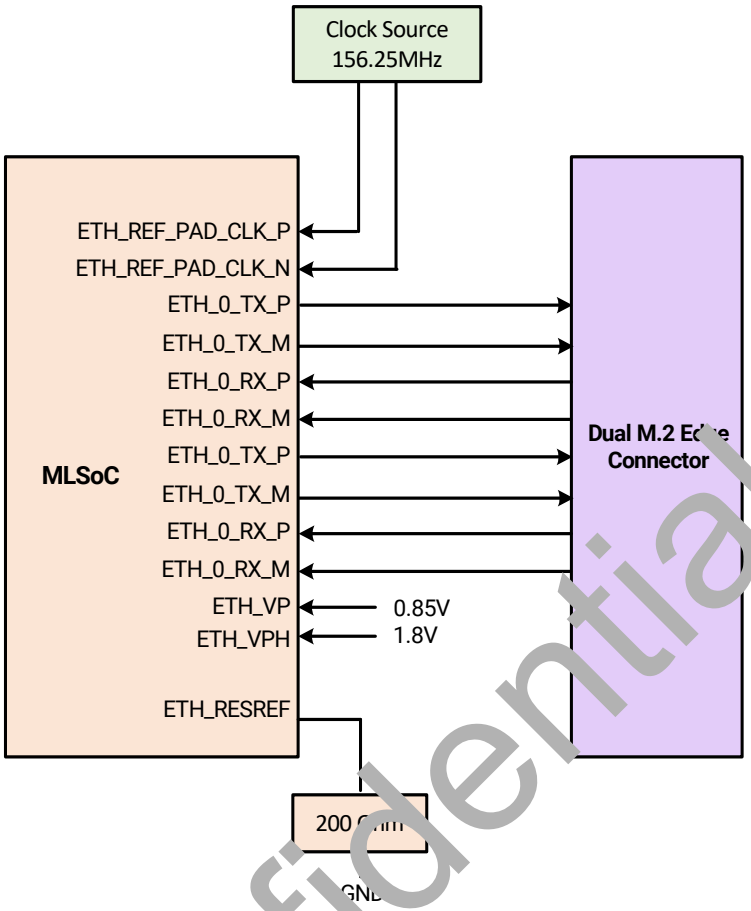

Figure 2-7. MLSoC Ethernet Interface

Table 2-9. shows the Ethernet interface pin-outs.

Table 2-9. Ethernet Interface Pin-outs

Interface Signals		IO Standards
MLSoC	Edge Connector/Oscillator	
ETH_REF_PAD_CLK_P	ETH_REFCLK_156.250MHz_P	Ethernet REF clock +ve
ETH_REF_PAD_CLK_N	ETH_REFCLK_156.250MHz_N	Ethernet REF clock -ve
ETH_0_TX_P	ETH1_TX_P	Ethernet1 Transmitter +ve
ETH_0_TX_M	ETH1_TX_N	Ethernet1 Transmitter -ve
ETH_0_RX_P	ETH1_RX_P	Ethernet1 Receiver +ve
ETH_0_RX_M	ETH1_RX_N	Ethernet1 Receiver -ve
ETH1_TX_P	ETH2_TX_P	Ethernet2 Transmitter +ve
ETH1_TX_M	ETH2_TX_N	Ethernet2 Transmitter -ve
ETH1_RX_P	ETH2_RX_P	Ethernet2 Receiver +ve
ETH1_RX_M	ETH2_RX_N	Ethernet2 Receiver -ve

2.4.6 MLSoC UART Interfaces

- Five UART controllers are present in the MLSoC device. UARTB is used for Troot boot and UART2 is used for Linux boot functions. The remaining MLSoC UART ports are not utilized on this board design.
- The Level translator with P/N TXS0102DCT are used to convert the MLSoC UART signals to a 3.3 IO level.

Figure 2-8. shows the UART interfaces of the MLSoC.

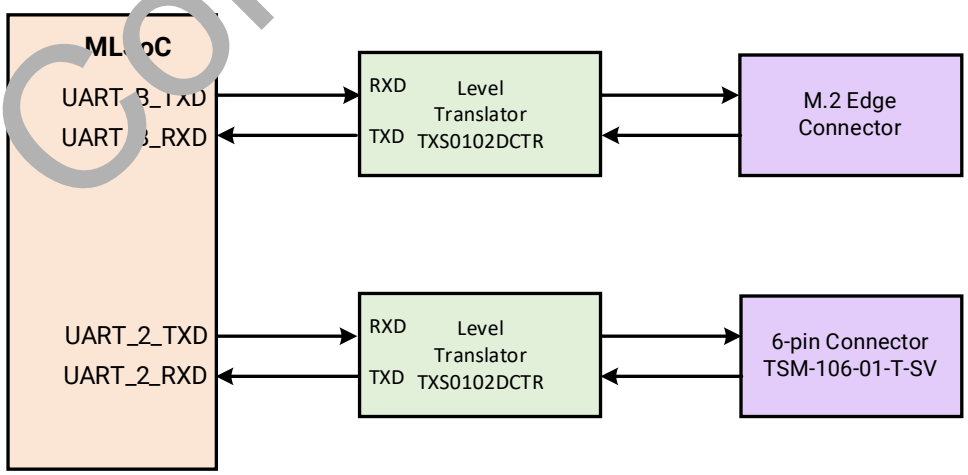

Figure 2-8. MLSoC UART Interface

Table 2-10. shows the UART interface pin-outs.

Table 2-10. UART Interface Pin-outs

Interface Signals		IO Standards
MLSoC	**Signal Name**	
UART_TX	TXD	OUTPUT, 3.3V
UART_RX	RXD	INPUT, 3.3V

Table 2-11. shows the UART connector pin-outs.

Table 2-11. UART Connector Pin-outs

6-pin Connector Pin		Signal Type
Pin No.	**Signal Name**	
1	GND	Ground
2	NC	Not Connected
3	NC	Not Connected
4	TXD	Transmit Asynchronous Data output
5	RXD	Receive Asynchronous Data input
6	NC	Not Connected

2.4.7 Joint Test Action Group (JTAG) Interface

- One standard JTAG interface and one Test JTAG interface are present in the MLSoC. In Dual M.2 Board, Test JTAG connector is not populated.
- Normally the JTAG interface is used for programming/debugging the MLSoC using an external programmer device.
- Since the MLSoC JTAG signal IO level is 1.8V, a JTAG buffer device with P/N SN74LVC244ARWP is used for the JTAG signals for the programmer device.
- One separate 14-pin connector with P/N: 15916142 is used for the JTAG interface as well as the JTAG test signals interface.

Figure 2-9. shows a representation of both normal JTAG and Test JTAG interfaces of the MLSoC.

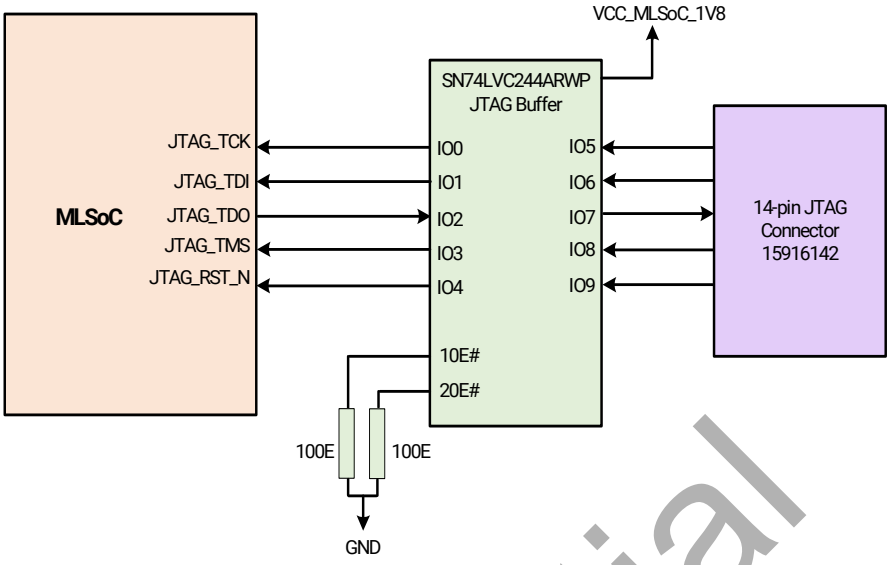

Figure 2-9. MLSoC JTAG Interface

Table 2-12. shows the MLSoC JTAG pin-outs.

Table 2-12. MLSoC JTAG Pin-outs

Signal Name	JTAG Pin	IO Logic
TCK	1A2/1Y2	INPUT, 1.8V
TDI	1A3/1Y3	INPUT, 1.8V
TDO	2A1/2Y1	OUTPUT, 1.8V
TMS	1A1/1Y1	INPUT, 1.8V
RST_N	1A4/1Y4	OUTPUT, 1.8V

Table 2-13. shows the MLSoC test JTAG pin-outs.

Table 2-13. MLSoC JTAG Connector Pin-outs

Pin Number	Signal Name	Description
5	VCC	Voltage
1	TMS	Test Mode Select
11	TCK	Test Clock
7	TDO	Test Data Out
3	TDI	Test Data In
2	TRSTn	RESET
8,10,12	GND	Ground
4,6,9,13,14	NC	No connect

2.4.8 MLSoC SPI-8 Interface

- One quad and two Octal SPI controllers are present in MLSoC device, namely SPIB, SPI0, and SPI1.
- The SPI0 controller from the MLSoC is used to connect the SPI flash, where the initial boot loader is present and the MLSoC boots up after power on by reading this flash.
- For the MLSoC Dual M.2 Board, both the SPIB and the SPI1 controller bus signals are not connected to any device.
- A 128-Mbit Quad SPI flash IC with P/N W25Q128JWSIQ is used as boot ROM. This IC is an 8-bit SPI with a maximum clock rate of 133MHz.
- A 10 POS 100Mils header connector with P/N 10129381-910004BLF is used for flashing the SPI through an Aardvark I2C/SPI Host Adapter.

Figure 2-10. shows the MLSoC SPI-8 interface.

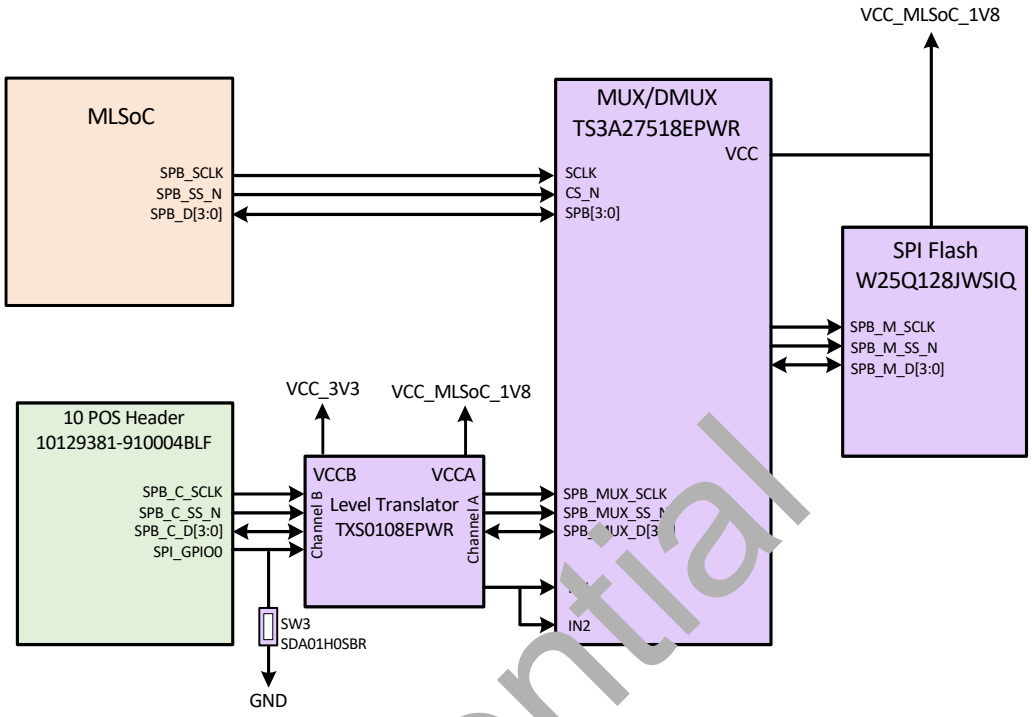

Figure 2-10. MLSoC SPI-8 Interface

Table 2-14. shows the MLSoC Quad SPI-8 Interface Pin-outs.

Table 2-14. MLSoC Quad SPI Programming Header Pin-outs

MLSoC Signal Name	SPI Flash Signal Name	Description
J5.1	RESET_EXT	Externally controlled RESET Input
J5.3	SPI_GPIO0	GPIO to control MUX select line
J5.4	SPB_C_D2	SPI Data 2 Signal
J5.5	SPB_C_D1	SPI Data 1 Signal
J5.6	SPB_C_D3	SPI Data 3 Signal
J57	SPB_C_SCLK	SPI Clock Signal
J5.8	SPB_C_D0	SPI Data 0 Signal
J5.2, J5.9, J5.10	GND	Ground ne

2.4.9 GPIO Interface

- 32 GPIO signals are available in the MLSoC device.
- Only 10 GPIOs are used in the MLSoC Dual M.2 Board design; the remaining GPIOs are NC.
- 4x of GPIOs are connected to DIP switch, SW2, for software configuration.
- 6x of GPIOs are connected to the M.2 edge connector interface, J3.
- GPIO0 and GPIO1 are used for the PCIE_WAKE_N and the PCIE_CLKREQ functions, respectively.

Figure 2-11. shows the MLSoC GPIO interface.

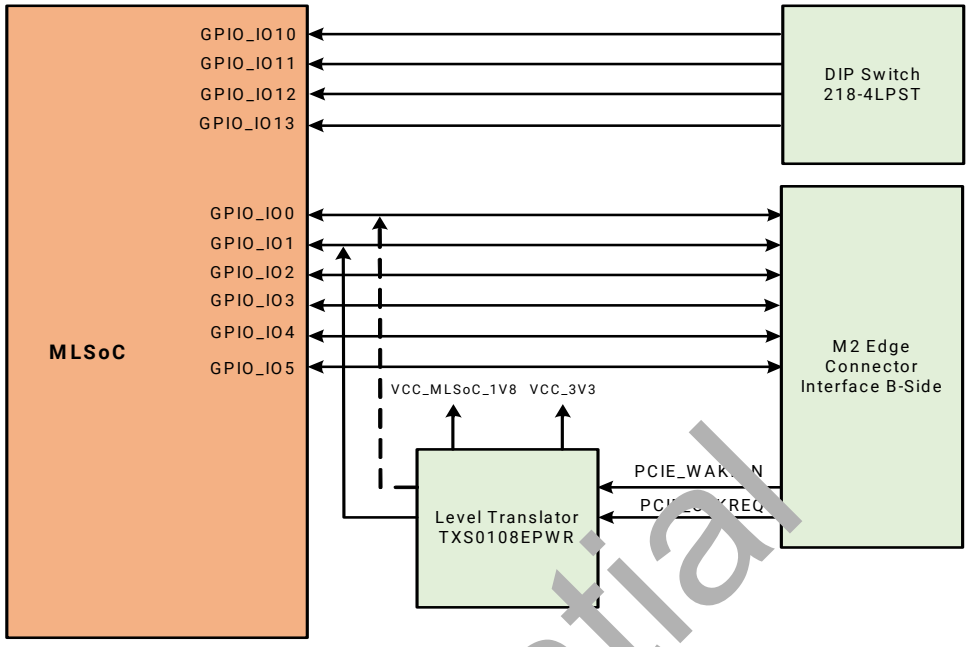

Figure 2-11. MLSoC GPIO Interface

Table 2-15. shows the MLSoC GPIO Interface Pin-outs.

Table 2-15. MLSoC GPIO Interface Pin-outs.

Pin Number	Signal Name - MLSoC	Description
J4.30/J3.54	ML_GPIO0	PCIE_WAKE_N
J4.28/3.52	ML_GPIO1	PCIE_CLKREQ
J4.26	ML_GPIO2	General Purpose IO
J4.24	ML_GPIO3	General Purpose IO
J4.22	ML_GPIO4	General Purpose IO
J4.20	ML_GPIO5	General Purpose IO
SW2.8	ML_GPIO10	General Purpose IO
SW2.7	ML_GPIO11	General Purpose IO
SW2.6	ML_GPIO12	General Purpose IO
SW2.5	ML_GPIO13	General Purpose IO

2.4.10 PCIe Interface

- 1x PCIe Gen 4.0 x8 PHY controller is present in MLSoC device.
- The PCIe Gen 4.0 supports per lane link speeds of up to 16Gbps.
- The PCIe PHY supports as an endpoint when in PCIe mode.
- On board 100MHz oscillator with P/N 510DBA100M000AAG is used as a PCIe reference clock (optional).
- The voltage requirement for PCIe PHY Controller is as follows:
  - PCIe_VP = 0.85V
  - PCIe VPH = 1.8V
- The REFRES Pin of the PHY controller is for calibrating the termination resistance of the TX and RX lines is connected to a 200-ohm ±1% precision resistor.
- In the MLSoC Dual M.2 Board all of the PCIe lanes are connected to the board edge connector and the board operates only as an end point acceleration board.
- Two standard M.2 75-pin board edge connections U3 and U4, are used to interface the MLSoC Dual M.2 Board with a motherboard.

Figure 2-12. shows the PCIe Gen 4.0 interface functional block diagram.

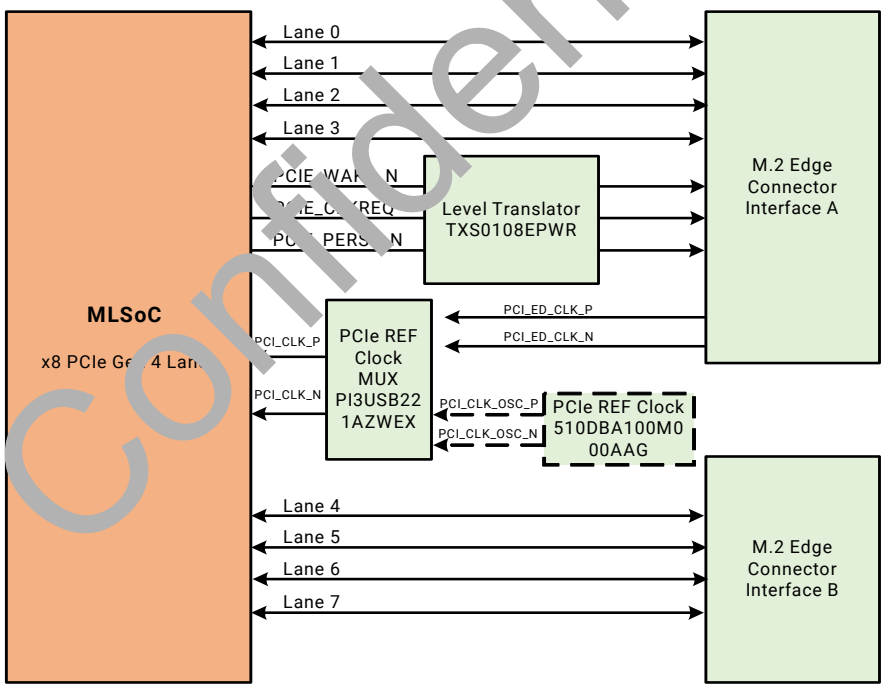

Figure 2-12. x8 PCIe Gen 4.0 Interface Functional Block Diagram

Table 2-16. shows the MLSoC PCIe Gen 4.0 x8 Dual M.2 Edge Connector pin-outs.

Table 2-16. MLSoC PCIe Gen 4.0 x8 Dual M.2 Edge Connector Pin-outs

Edge Connector Pin Number	Edge Connector Signal Name	Signal Name	Description
J3.55	PCIE_CLK_QO_C_P	PCI_ED_CLK_P	IN, PCIe Reference clock+
J3.53	PCIE_CLK_QO_C_N	PCI_ED_CLK_N	IN, PCIe Reference clock-
J3.49	PCIe_RX0_P	PCIE_RX_P[7]	IN, Lane 7 Receive Data+
J3.47	PCIe_RX0_N	PCIE_RX_N[7]	IN, Lane 7 Receive Data-
J3.43	PCIe_TX0_P	PCIE_TX_P[7]	OUT, Lane 7 Transmit Data+
J3.41	PCIe_TX0_N	PCIE_TX_N[7]	OUT, Lane 7 Transmit Data-
J3.37	PCIe_RX1_P	PCIE_RX_P[6]	IN, Lane 6 Receive Data+
J3.35	PCIe_RX1_N	PCIE_RX_N[6]	IN, Lane 6 Receive Data-
J3.31	PCIe_TX1_P	PCIE_TX_P[6]	OUT, Lane 6 Transmit Data+
J3.29	PCIe_TX1_N	PCIE_TX_N[6]	OUT, Lane 6 Transmit Data-
J3.25	PCIe_RX2_P	PCIE_RX_P[5]	IN, Lane 5 Receive Data+
J3.23	PCIe_RX2_N	PCIE_RX_N[5]	IN, Lane 5 Receive Data-
J3.19	PCIe_TX2_P	PCIE_TX_P[5]	OUT, Lane 5 Transmit Data+
J3.17	PCIe_TX2_N	PCIE_TX_N[5]	OUT, Lane 5 Transmit Data-
J3.13	PCIe_RX3_P	PCIE_RX_P[4]	IN, Lane 4 Receive Data+
J3.11	PCIe_RX3_N	PCIE_RX_N[4]	IN, Lane 4 Receive Data-
J3.07	PCIe_TX3_P	PCIE_TX_P[4]	OUT, Lane 4 Transmit Data+
J3.05	PCIe_TX3_N	PCIE_TX_N[4]	OUT, Lane 4 Transmit Data-
J4.49	PCIe_RX4_P	PCIE_RX_P[3]	IN, Lane 3 Receive Data+
J4.47	PCIe_RX4_N	PCIE_RX_N[3]	IN, Lane 3 Receive Data-
J4.43	PCIe_TX4_P	PCIE_TX_P[3]	OUT, Lane 3 Transmit Data+
J4.41	PCIe_TX4_N	PCIE_TX_N[3]	OUT, Lane 3 Transmit Data-
J4.37	PCIe_RX5_P	PCIE_RX_P[2]	IN, Lane 2 Receive Data+
J4.35	PCIe_RX5_N	PCIE_RX_N[2]	IN, Lane 2 Receive Data-
J4.31	PCIe_TX5_P	PCIE_TX_P[2]	OUT, Lane 2 Transmit Data+
J4.29	PCIe_TX5_N	PCIE_TX_N[2]	OUT, Lane 2 Transmit Data-
J4.25	PCIe_RX6_P	PCIE_RX_P[1]	IN, Lane 1 Receive Data+
J4.23	PCIe_RX6_N	PCIE_RX_N[1]	IN, Lane 1 Receive Data-
J4.19	PCIe_TX6_P	PCIE_TX_P[1]	OUT, Lane 1 Transmit Data+
J4.17	PCIe_TX6_N	PCIE_TX_N[1]	OUT, Lane 1 Transmit Data-

Table 2-16. MLSoC PCIe Gen 4.0 x8 Dual M.2 Edge Connector Pin-outs (continued)

Edge Connector Pin Number	Edge Connector Signal Name	Signal Name	Description
J4.13	PCIe_RX7_P	PCIE_RX_P[0]	IN, Lane 0 Receive Data+
J4.11	PCIe_RX7_N	PCIE_RX_N[0]	IN, Lane 0 Receive Data-
J4.07	PCIe_TX7_P	PCIE_TX_P[0]	OUT, Lane 0 Transmit Data+
J4.05	PCIe_TX7_N	PCIE_TX_N[0]	OUT, Lane 0 Transmit Data-

Chapter 3
Clock Requirements

3.1 Clock Requirements

The clock requirements of the MLSoC Dual M.2 Board is provided in **Table 3-1.**

Table 3-1. Dual M.2 Board - Clock Requirements

Item No.	Oscillator Frequency	Clock Source	Frequency Stability/Tolerance	Device	Interface
1	100MHz	Oscillator (optional)	+/-30ppm	MLSoC	PHY reference clock (optional)
2	33MHz	Oscillator	+/-10ppm	MLSoC	Used as MLSoC reference clock
3	32.768KHz	Crystal	+/-20ppm	MLSoC	RTC reference clock
4	156.25MHz	Oscillator	+/-50ppm	MLSoC	Ethernet MAC Reference clock

Chapter 4
Power and Reset

This chapter describes the following topics:

- The power requirements
- The Buck regulator for the MLSoC core voltage of 0.85V@40A
- The Buck regulator for the LPDDR4 Controller VDDQ voltage and LPDDR4 IC 1.1V@2.5A
- The Buck regulator for the MLSoC IO voltages, the LPDDR4 VDD, and the eMMC VDDQ 1.8@2.4A
- The 5V Boost regulator to supply the VDD pin of 0.85V buck regulator
- The system reset

4.1 Power Requirements

The board has different power inputs for different configurations. The main power input is connected to the regulator circuitry to generate multiple power requirements for the MLSoC and all on-board interface circuitry.

4.1.1 Circuit Protection

To suppress high-frequency noise, thereby reducing the risk of equipment malfunction, the board includes multiple EMI filters and ferrite beads, where necessary.

4.1.2 Power Tree

The power supplies required for the MLSoC and memory interfaces are generated from regulators that are separate from the regulators for generating the power supply for other interface circuits of the board. The power supplies are described below.

- 3.3V main supply is provided by the M.2 interface of the host machine. Three different Buck regulators are used for the Dual M.2 Board power supplies:
  - 3.3V main supply is provided by either the PCIe base board or the ethernet board.
  - A Buck Regulator for Core Voltage 0.85V
  - A Buck Regulator for IO voltage, LPDDR4 VDD1, and the eMMC VDD1 supply of 1.8V
  - A Buck Regulator for the LPDDR4 memory devices and the LPDDR4 Controller VDDQ Supply of 1.1V
- A IO voltage is ramped up before the core voltage of MLSoC.
- The multiple buck regulators and a PMIC is used for both the power supply of other interfaces on the board.
- The 0.85V power rail is using a regulator with P/N TPS548D21RVFT. The 1.8V and the 1.1V power rails are using their own NCP1599 regulator.

4.2 Buck Regulator for MLSoC Core Voltage 0.85V @ 40A

- Part Number: TPS548D21RVFT
- Package: LQFN-CLIP
- Operating Temperature: —40C to +125°C

TPS548D21RVFT is a fully integrated buck converter with synchronous MOSFET switches and high-performance inductors. This IC will convert 3.3V to 0.85V@40A and is used for power supply pins for the internal core logic of the MLSoC. A wide range of input from 1.5V to 16V can be supplied to this IC. Since IO voltage of MLSoC needs to be ramped up before the core voltage, the CTRL pin of this IC is connected to the IO voltage regulator output.

4.3 Buck Regulator for LPDDR4 Controller VDDQ Voltage and LPDDR4 IC 1.1V@2.5A

- Part Number: NCP1599MNTWG
- Package: DFN6
- Operating Temperature: —40°C to +85°C

This buck regulator is used to generate 1.1V@2.5A from the 3.3V regulated supply. The output voltage is supplied to MLSoC LPDDR4 VDD2, VDDQ and LPDDR4 Controller VDDQ Pins. This IC comes with integrated MOSFETs. Also, this device has a wide input range from 3V to 5.5V.

4.4 Buck Regulator for MLSoC IO Voltages, LPDDR4 VDD, eMMC VDDQ 1.8@ 2.4A

- Part Number: NCP1599MNTWG
- Package: DFN6
- Operating Temperature: —40°C to +85°C

This buck regulator is used to generate 1.8V@2.4A from the 3.3V regulated supply. The output voltage is supplied for MLSoC IO voltage, LPDDR4 VDD1 and other voltages required for different interface controllers. This IC comes with integrated MOSFETs. Also, this device has a wide input range from 3V to 5.5V.

4.5 Boost Regulator to Supply VDD Pin of 0.85V Buck Regulator

- Part Number: XC9140A501MR-G
- Package: SC-74A, SOT-753
- Operating Temperature: —40°C to +85°C

This buck regulator is used to generate the 5V from 3.3V regulated supply. The output voltage of this regulator is supplied to the VDD pin of the 0.85V buck regulator. Since there is no 5V voltage source in this design, a separate boost is used to provide the required voltage to the controller power supply of the 0.85V buck regulator.

4.6 System Reset

The Power ON reset functionality of the MLSoC Dual M.2 Board is implemented in one of two ways:

- By asserting the PERST# via the PCIe bus from the M.2 interface
- By pressing the hardware reset button, SW3, on the MLSoC Dual M.2 Board.

NOTE!

Board Power up will be completed and it will come out of reset. Once the MLSoC chip is out of reset, the MLSoC Dual M.2 Board will boot. The PHY settings need to be applied to the PCIe PHY before the PERST # de-asserts.
Figure 4-1. shows the system reset.

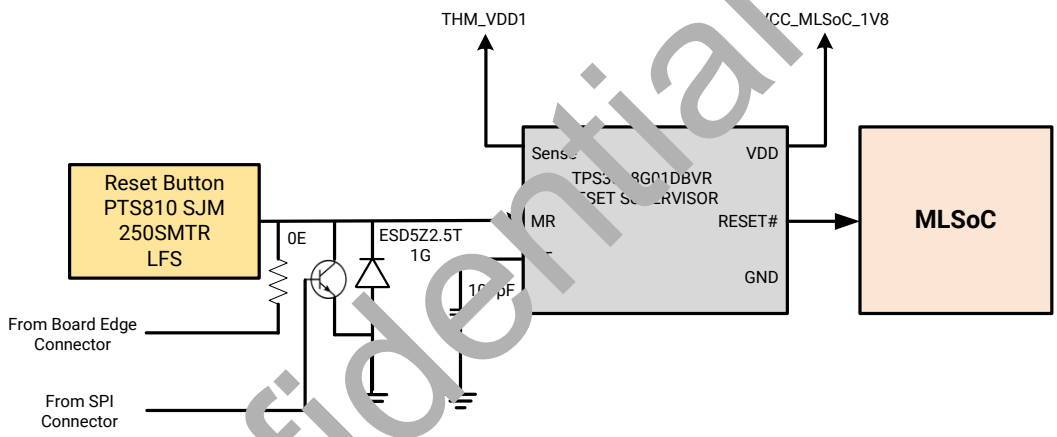

Figure 4-1. System Reset

- An on-board reset switch with P/N PTS810 SJM 250 SMTR LFS is used to reset the board.
- An ESD protection diode with P/N ESD5Z2.5T1G is used to protect MLSoC from high surges.
- The capacitor in the CT pin is used to select the RESET delay time.

Chapter 5
Operation and Maintenance

This chapter describes the following topics:

- LED requirements
- Test points

5.1 LED Requirements

The LED features as shown in **Table 5-1.** are supported on the MLSoC Dual M.2 Board.

Table 5-1. LED Requirements Supported on the MLSoC Dual M.2 Board

Item No.	Signal	LED Color	Status
1	RESET_IN_N	RED	MLSoC reset

5.2 Test Points

Depending on the space availability, test points are provided (wherever necessary) for voltages and ground.

Chapter 6
PCB & Packaging

This chapter describes the following topics:

- PCB size and thickness
- Board layer description

6.1 PCB Dimensions

- PCB Size (Dual M.2 form factor): 110mm (L) × 46mm (W)
- PCB Thickness: 0.8mm (H)

6.2 Board Layer Description

The PCB stack-up includes 10 layers and the layer sequence is as shown in **Table 6-1.**

Table 6-1. PCB 10 Layer Stack-up

Item No.	Layer Description
1	TOP
2	GND1
3	SIG1
4	GND2
5	SIG2
6	VCC1
7	GND3
8	SIG3
8	GND4
10	BOTTOM

Chapter 7
Signal and Power Integrity Analysis

Signal and power integrity are major factors which decide the performance and functionality of a device. This chapter describes the following topics:

- Pre-layout Signal Integrity (SI) Analysis
- Post-layout Signal Integrity Analysis
- Power Integrity (PI) Analysis
- Thermal Analysis

7.1 Pre-Layout Signal Integrity Analysis

Pre-layout signal integrity analysis is done once the placement is finalized and before starting the routing of the signals. The main purpose of the pre-layout analysis is to develop design constraints.

7.2 Post-Layout Signal Integrity Analysis

Post-layout SI analysis is done after the layout design and feedback is implemented. The following are the major analyses which are carried out for PCIe and DDR interfaces. The post-layout SI analysis verifies the compliance to the design constraints.

- *S-parameter Analysis* (Insertion loss, Return Loss, FEXT & NEXT): The S-parameter simulation is a well-suited tool to characterize complex circuits at high frequency to ensure signal integrity. S-parameter simulation is a type of Alternating Current (AC) simulation that represents the small-signal behavior of the device at the given temperature, bias conditions, and input signals.
- *Crosstalk Analysis*: Cross talk occurs when energy in one signal couples onto another signal. To avoid this, signal spacing, voltage swing, distance to ground, typical cross talk and typical route length are analyzed.
- *Eye Analysis*: Eye diagrams help to identify the signal quality and the noise margins. This helps in identifying the noise sources and in improving the signal quality.

7.3 Power Integrity Analysis

Post-layout PI analysis is done after the layout design and feedback has been implemented.

- *IR (Intermediate Resistance) Drop Analysis*: There are many inter-dependent factors that can impact IR drop including signal flow path, trace geometry, thermal effect, impedance matching, and count and size of via.

7.4 Thermal Analysis

Board level thermal analysis is done for ambient temperature and feedback is implemented. This helps in identifying temperature dense areas on the board for ambient temperature. The result of this analysis is considered for the SiMa.ai MLSoC Dual M.2 Board heat sink design.

Chapter 8
Certification Data

This chapter provides certification data and describes the summary of emissions and immunity test results.

The Equipment Under Test (EUT) was configured for testing in accordance with requirements of the EN 55032: 2015/A11: 2020, BS EN 55032:2015+A1:2020, and EN/BS EN 55035:2017/A11:2020 standards.

8.1 Summary of Test Results

8.1.1 Emissions

Table 8-1. shows the Emissions results.

Table 8-1. Emissions Results

Standard	Test Description	Result
EN/BS EN 55032 Section A.3	Conducted Emissions	Note[a]
EN/BS EN 55032 Section A.2	Radiated Emissions	Compliant with Class A Limits
EN/BS EN 61000-3-2	Harmonic Current Emissions	Note[a]
EN/BS EN 61000-3-3	Voltage Fluctuation and Flickers	Note[a]

a. The EUT was Direct Current (DC) powered.

NOTE! Signal Line/data cables were not longer than 3m in length.

Table 8-2. shows the Immunity results.

Table 8-2. Immunity Results

Standard	Test Description	Result
EN/BS EN 55035 Section 4.2.1	Electrostatic Discharges EN/BS EN 61000-4-2	Compliant
EN/BS EN 55035 Section 4.2.2.2	Continuous Radiated Disturbances EN/BS EN 61000-4-3	Compliant
EN/BS EN 55035 Section 4.2.4	Electrical Fast Transients EN/BS EN 61000-4-4	Note[a]
EN/BS EN 55035 Section 4.2.5	Surges EN/BS EN 61000-4-5	Note[a]
EN/BS EN 55035 Section 4.2.2.3	Continuous Conducted Disturbances EN/BS EN 61000-4-6	Note[a]
EN/BS EN 55035 Section 4.2.3	Power-frequency Magnetic Fields EN/BS EN 61000-4-8	Compliant
EN/BS EN 55035 Section 4.2.6	Voltage Dips and Interruptions EN/BS EN 61000-4-11	Note[a]

a. The EUT was DC powered.

NOTE! Signal Line/data cables were not longer than 3m in length.
A complete Certification Report (*SiMa_2301133-2- Final.pdf*) is available from SiMa.ai.
Please contact SiMa.ai to get a copy of this report.

Chapter 9
Environmental and Compliance Specifications

This chapter describes the following topics:

- Environmental requirements
- Environmental specifications
- EMI/EMC and other compliance

9.1 Environmental Requirements

The operating temperature range of the MLSoC Dual M.2 Board is 0°C to 70°C (commercial grade) and —40°C to +85°C (industrial grade).

9.2 Environmental Specifications

The MLSoC Dual M.2 Board uses thermal conduction for its cooling method.

9.3 EMI/EMC and Other Compliance

The EMI/EMC (Electromagnetic Interference/Electromagnetic Compatibility) design guidelines need to be followed as per the device datasheet. Also follow the general PCB design guidelines to avoid the EMI/EMC-related issues.

Follow these precautions during the design:

1. Try to use Switching Regulators with integrated/built in inductor.
2. Use EMI/EMC common mode filters and power filters at the power supply.
3. The power plane routing should not be zigzagged. The power plane needs to be straight from the source to the sink.
4. All the power must have an immediate ground reference.

Chapter 10
Support

If you have questions, please contact our support team in one of the following two ways:

- Submit your request at https://simaai.zendesk.com
- Email: support@sima.ai

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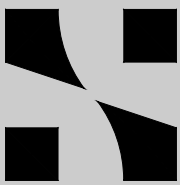

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